50th Best Paper and Presentation Nominations

Research Track Best Paper Nominees:

9.1 — Aging-Aware Compiler-Directed VLIW Assignment for GPGPU Architectures

Speaker: Abbas Rahimi-Univ. of California at San Diego, La Jolla, CA
Authors: Abbas Rahimi-Univ. of California at San Diego, La Jolla, CA
Luca Benini-Univ. di Bologna, Bologna, Italy
Rajesh Gupta-Univ. of California at San Diego, La Jolla, CA

12.4 — An ATE Assisted DFD Technique for Volume Diagnosis of Scan Chains

Speaker: Subhadip Kundu-Indian Institute of Technology, Kharagpur, India
Authors: Subhadip Kundu-Indian Institute of Technology, Kharagpur, India
Santanu Chattopadhyay-Indian Institute of Technology, Kharagpur, India
Indranil Sengupta-Indian Institute of Technology, Kharagpur, India
Rohit Kapur-Synopsys, Inc., Mountain View, CA

16.1 — Proactive Circuit Allocation in Multiplane NoCs

Speaker: Ahmed Abousamra-Univ. of Pittsburgh , Pittsburgh, PA
Authors: Ahmed Abousamra-Univ. of Pittsburgh , Pittsburgh, PA
Alex K. Jones-Univ. of Pittsburgh , Pittsburgh, PA
Rami Melhem-Univ. of Pittsburgh , Pittsburgh, PA

18.6 — A High-Level Synthesis Flow for the Implementation of Iterative Stencil Loop Algorithms on FPGA Devices

Speaker: Alessandro Antonio Nacci-Politecnico di Milano, Milan, Italy
Authors: Alessandro Antonio Nacci-Politecnico di Milano, Milan, Italy
Vincenzo Rana-Politecnico di Milano, Milan, Italy
Ivan Beretta-Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland
Francesco Bruschi-Politecnico di Milano, Milan, Italy
David Atienza-Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland
Donatella Sciuto-Politecnico di Milano, Milan, Italy

24.1 — ABCD-L: Approximating Continuous Linear Systems Using Boolean Models

Speaker: Aadithya Karthik-Univ. of California, Berkeley, CA
Authors: Aadithya Karthik-Univ. of California, Berkeley, CA
Jaijeet Roychowdhury-Univ. of California, Berkeley, CA

31.1 — Scalable Vectorless Power Grid Current Integrity Verification

Speaker: Zhuo Feng-Michigan Technological Univ., Houghton, MI
Author: Zhuo Feng-Michigan Technological Univ., Houghton, MI

32.4 — Spacer-Is-Dielectric-Compliant Detailed Routing for Self-Aligned Double Patterning Lithography

Speaker: Yuelin Du-Univ. of Illinois at Urbana-Champaign, Urbana, IL
Authors: Yuelin Du-Univ. of Illinois at Urbana-Champaign, Urbana, IL
Martin D. F. Wong-Univ. of Illinois at Urbana-Champaign, Urbana, IL
Qiang Ma-Synopsys, Inc., Mountain View, CA
Hua Song-Synopsys, Inc., Mountain View, CA
James Shiely-Synopsys, Inc., Hillsboro, OR
Gerard Luk-Pat-Synopsys, Inc., Mountain View, CA
Alexander Miloslavsky-Synopsys, Inc., Mountain View, CA

37.2 — Rapid Exploration of Processing and Design Guidelines to Overcome Carbon Nanotube Variations

Speaker: Gage Hills-Stanford Univ., Stanford, CA
Authors: Gage Hills-Stanford Univ., Stanford, CA
Jie Zhang-Google, Inc., Mountain View, CA
Charles Mackin-Massachusetts Institute of Technology, Cambridge, MA
Max Shulaker-Stanford Univ., San Mateo, CA
Hai Wei-Stanford Univ., Stanford, CA
H.S. Philip Wong-Stanford Univ., Stanford, CA
Subhasish Mitra-Stanford Univ., Stanford, CA

Designer Track Best Presentation Nominees

5.1 — Using Formal Verification to Replace Mainstream Simulation

Speaker: Erik Seligman-Intel Corp., Hillsboro, OR
Authors: Erik Seligman-Intel Corp., Hillsboro, OR
Brandon J. Smith-Intel Corp., Hillsboro, OR

5.5 — Automatic Verification of Floating Point Units

Speaker: Udo Krautz-IBM Systems and Technology Group, Boeblingen, Germany
Authors: Udo Krautz-IBM Systems and Technology Group, Boeblingen, Germany
Viresh Paruthi-IBM Systems and Technology Group, Austin, TX
Anand B. Arunagiri-IBM Server and Technology Group, Bangalore, India
Sujeet Kumar-IBM Server and Technology Group, Bangalore, India

6.2 — Design of Optimal Closed Loop Controller and OS Scheduler for Dynamic Energy Management in Heterogeneous Multicore Processors

Speaker: Vinay Hanumaiah-Arizona State Univ., Tempe, AZ
Authors: Vinay Hanumaiah-Arizona State Univ., Tempe, AZ
Digant Desai-Arizona State Univ., Tempe, AZ
Sarma Vrudhula-Arizona State Univ., Tempe, AZ

10.1 — Advanced Model-Based Hotspot Fix Flow for Layout Optimization with Genetic Algorithm

Speaker: Shuhei Sota-Toshiba Microelectronics Corp., Yokohama, Japan
Authors: Shuhei Sota-Toshiba Microelectronics Corp., Yokohama, Japan
Taiga Uno-Toshiba Corp., Yokohama, Japan
Masanari Kajiwara-Toshiba Corp., Yokohama, Japan
Chikaaki Kodama-Toshiba Corp., Yokohama, Japan
Hirotaka Ichikawa-Toshiba Microelectronics Corp., Kawasaki, Japan
Ryota Aburada-Toshiba Corp., Yokohama, Japan
Toshiya Kotani-Toshiba Corp., Yokohama, Japan
Kei Nakagawa-Toshiba Microelectronics Corp., Kawasaki, Japan
Tamaki Saito-Toshiba Microelectronics Corp., Kawasaki, Japan

10.2 — Use of Hierarchical Design Methodologies in Global Infrastructure of the POWER7+ Processor

Speaker: Brian Veraa-IBM Systems and Technology Group, Austin, TX
Authors: Brian Veraa-IBM Systems and Technology Group, Austin, TX
Ryan Nett-IBM Systems and Technology Group, Austin, TX
Ryan M. Kruse-IBM Systems and Technology Group, Austin, TX

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