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Density functional theory based analysis of the origin of traps at the InAs/Si hetero-interface

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The growth of III-V semiconductors on Si generates defects at the III-V/Si interface which are known to degrade the performance of electronic devices where this interface is an active region. This paper presents a density functional theory based analysis of the InAs/Si interface with the aim to find the origin of traps at this interface. The optimized structure is obtained by structural minimization and is compared with a filtered Transmission Electron Microscopy image from the literature. The good qualitative agreement between the two results validates the atomic model of the InAs/Si interface. Electronic structural calculations are performed on the geometrically optimized InAs/Si slab to identify the interface trap levels. The study reveals that the InAs/Si interface traps originate from unsaturated orbitals present on Arsenic interface atoms. The saturation of the unsaturated As atoms by H or S is able to passivate the interface and to reduce the D_{it} . *Published by AIP Publishing.*

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In the past few decades, the exponential scaling of Si Complementary MOSFETs (CMOS) led to significant improvements in speed, energy consumption, and device density of integrated circuits (ICs). These advances, however, are saturating due to the intrinsic physical constraints of Si as a semiconductor. To circumvent these limitations, integration of various III-V materials on Si has been proposed.^{1,2} Furthermore, monolithic integration of optoelectronic devices such as lasers and light emitting diodes (LEDs) on ICs for on-chip photonics may be achieved by the growth of III-V on Si.^{3,4} This creates a III-V/Silicon heterojunction which is known to exhibit a high defect density due to the large lattice mismatch between Si and many III-V semiconductors. These defects give rise to interface traps which degrade the device performance. The investigation into the origin and nature of such interface traps using *ab-initio* atomistic modeling is a useful first step in mitigating their detrimental impact.

In our earlier work,⁵ physics-based technology-computer-aided-design (TCAD) simulation of InAs/Si heterojunction nanowire Tunnel Field Effect Transistors (TFETs) yielded good agreement with experimental temperature-dependent IV -plots⁶ only when the peak energy of the InAs/Si interface trap density (D_{it}) was chosen in the lower half of the InAs bandgap. This led to the presumption that the degradation of the TFET characteristics originates from D_{it} in the lower half of the gap. In this paper, an attempt is made to understand the origin of traps at the InAs/Si interface by performing electronic structure calculations using density functional theory (DFT). In the first step, structural minimization is performed on a relaxed InAs/Si interface to determine the atomic positions at the interface in a minimum energy configuration. This atomic structure at the interface is used in the next step in which electronic structural calculations are performed to find the origin of localized trap states at the interface.

Typically, Si(111) is used for the growth of III-V semiconductors due to the possibility of generating an

atomistically flat Si(111) surface by chemical etching. This technique had been employed for the growth of InAs on Si in the fabrication of the TFETs mentioned above. The Si(111) surface exhibits three types of reconstruction, namely, 1×1 , 1×2 , and 7×7 reconstruction.⁷ A surface treatment just before the growth typically involves Hydrogen Fluoride etching of a thin native oxide layer on the Si(111) surface. This and the wet hydroxide etching of Si result in a hydrogen-passivated Si(111) surface.⁸ Therefore, quasi-ideal 1×1 reconstructed H-passivated Si(111) is most likely to be present during the growth phase. Although the 7×7 -reconstructed Si(111) surface is the most stable one among all the reconstructions up to 850 °C, it involves a tremendous rearrangement of Si atoms at the surface. Therefore, it is not formed during wet etching of Si. Cleaving the Si crystal along (111) usually yields a metastable 2×1 reconstruction at room temperature. Yet, reports confirming the occurrence of a 2×1 reconstruction of Si during wet etching of Si or HF etching of oxide are unknown to the authors. Therefore, Si(111) with 1×1 reconstruction is assumed to be present at the InAs/Si interface in this study.

Due to the large lattice mismatch between InAs and Si (experimental value $\approx 11\%$), the pseudomorphic growth of lattice-matched InAs layers on the Si substrate is highly unfavorable. Therefore, in the atomistic simulations, defect creation is assumed to relax the strain in the first bilayer of InAs. This defect creation distorts the otherwise uniform placement of atoms at the interface. In the first step, structural minimization is performed to find the most favorable atomic structure at the InAs/Si interface using the Mixed Gaussian-Plane-Wave (GPW)¹⁰ based density functional theory (DFT) simulation package CP2K.^{11,12} Perdew-Burke-Ernzerhof (PBE) pseudopotentials were used along with a double-zeta valence + one polarization (DZVP) basis set¹³ for In, As, and Si atoms for modeling the structure. Structural minimization is performed on an InAs/Si slab consisting of 4 bilayers of relaxed InAs(111) stacked over 2 bilayers of relaxed Si(111) in the growth direction ((111)).

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Both InAs and Si are assumed to have a zinc-blende (ZB)/diamond crystal structure. The unit cell of the (111) slab of the zinc-blende (ZB) lattice is hexagonal with two (111) faces on top and bottom and four (110) faces on four vertical sides of the supercell. The lattice constants of InAs and Si are set to 6.247 Å and 5.478 Å, respectively, after structural minimization of the unit cell of the individual elements. Using the above lattice constants, 7 unit cells of InAs in $\langle 110 \rangle$ are nearly lattice matched to 8 unit cells of InAs in the $\langle 110 \rangle$ direction parallel to the interface. This lattice-matching results in 0.2% biaxial tensile strain in InAs instead of $\approx 12.5\%$ compressive strain that would be present if InAs is pseudomorphically grown on Si. Hence, a hexagonal supercell consisting of 7 and 8 unit cells of InAs and Si, respectively, along $\langle 110 \rangle$ (see Fig. 1) is simulated with periodic boundary conditions along the three directions. With this, the slab is padded with vacuum at the top and the bottom to ensure that periodic images of the InAs/Si slab along $\langle 111 \rangle$ do not interact. Growth of InAs on Si may take place by either an As termination at the InAs/Si interface or As incorporation in the monolayer of Si at the surface. The former mechanism leads to In-rich growth facet, while the latter one leads to As-rich growth facet along $\langle 111 \rangle$. In this work, the InAs(111) slab is assumed to be As-terminated at the interface. The top (111) surface of InAs and the bottom (111) surface of Si are hydrogen-passivated to avoid surface states. Initially, the relative position of the InAs slab with respect to the Si slab is determined by shifting the InAs slab along the three axes to minimize the energy of the structure. This position is then used for structural minimization. All atoms except those in the first two bilayers of InAs adjacent to the interface are constrained during structural minimization. Since bilayers of InAs are deposited over Si during the growth, InAs atoms are not expected to significantly alter the positions of Si atoms in the substrate. The root mean square (RMS) step and that of the RMS gradient and the maximum

gradient were chosen as convergence criteria. The convergence limits were set to their default values in CP2K.

In order to confirm the hypothesis that the mismatch strain is relaxed in the first bilayer of InAs, calculations were performed to find the critical height of pseudomorphous InAs on Si using the theory developed by People and Bean.⁹ Taking a slip distance (b -magnitude of Burger's vector) of 4 Å, it was found that the force on the dislocation line due to the misfit stress (F_H) of $\approx 12.5\%$ is greater than the tension in the dislocation line (F_D) for all values of the pseudomorphous layer thickness (h). This implies that a critical layer thickness (h_c) for which $F_H = F_D$ does not exist and a defect formation at the interface is more favorable for any h .

Additionally, structural minimization of lattice-matched strained InAs on the relaxed Si substrate was performed for up to 4 bilayers of InAs. The excess energy in the strained InAs (s-InAs)/Si system calculated by subtracting the energy of relaxed InAs (r-InAs), Si atoms in bulk, and H₂ in vacuum from the energy of the strained structure is plotted in Fig. 1(b). The systems with s-InAs have a higher excess energy compared to the r-InAs/Si system, suggesting that the latter is more favorable. Furthermore, structural minimization of the r-InAs/1 bilayer (BL) s-InAs/Si system is performed and the excess energy of the system is plotted. The atomic structure of the optimized system is shown in Fig. 1(c). The excess energy of this system is larger than that of r-InAs/Si. With more bilayers of strained InAs, the excess energy will further increase. This validates the hypothesis that r-InAs/Si is the most favorable structure.

The converged structure of atoms at the r-InAs/Si interface is shown in Fig. 1(a). The front view of the supercell in the (110) plane reveals that the periodic structure of InAs atoms at the interface remains more or less intact, except for the last unit cell in which the atoms undergo significant restructuring. From a closer look at the supercell, one finds that As atoms in the first monolayer are aligned to the atoms of the adjacent Si layer at the center of the cell. This alignment gradually impairs for As atoms away from the center. At the edge of the cell, the As and Si atoms are maximally misaligned, resulting in a non-uniform structure. Such a periodic disorder has been observed in the Transmission Electron Microscopy (TEM) images reported by Tomioka *et al.*¹⁴ The filtered TEM image of the difference between the predicted and the observed lattice constant in (110) at each atomic site as a fraction of the lattice constant of Si is shown in Fig. 2(b). For a quick comparison with this image, the difference between the atomic positions in the (110) plane before and after structural minimization of the simulated supercell is projected along the [0 0 1] direction and plotted in Fig. 2(c). The calculated atomic displacements show a good match with the filtered TEM image at the interface. As the atomic positions in bulk were constrained during structural minimization, the color is uniform in InAs and Si regions. The calculated positions correctly predict the periodic nature of the defects and the period. Thus, the derived atomic structure of the InAs/Si interface is a viable model to study the defects at the interface.

In the next step, electronic structural calculations have been performed using the DFT simulation package CP2K on an InAs/Si slab to find the origin of localized states at the

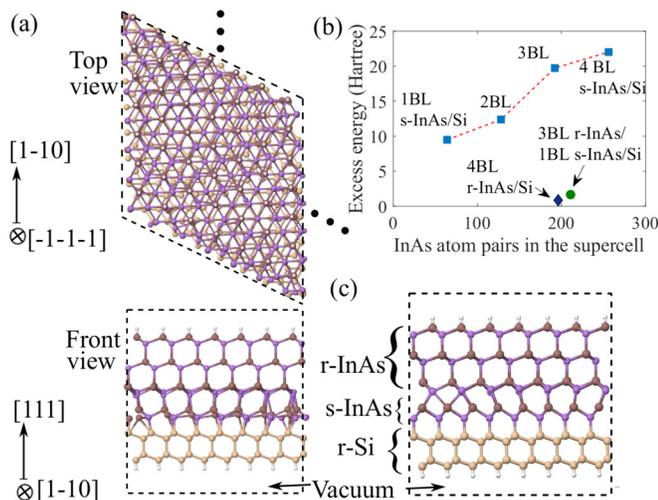


FIG. 1. (a) Unit cell of the InAs/Si slab after structural minimization. The top view shows the hexagonal shape of the unit cell with periodic boundaries, while the front view is the (110) view. (b) Excess energy in strained and relaxed InAs/Si slabs vs. InAs atom pairs. The number of Si atoms is kept constant among all the structures. (c) Unit cell of 3 bilayers (BL) of the relaxed-InAs/1 BL strained-InAs/Si slab after structural minimization ((110) view).

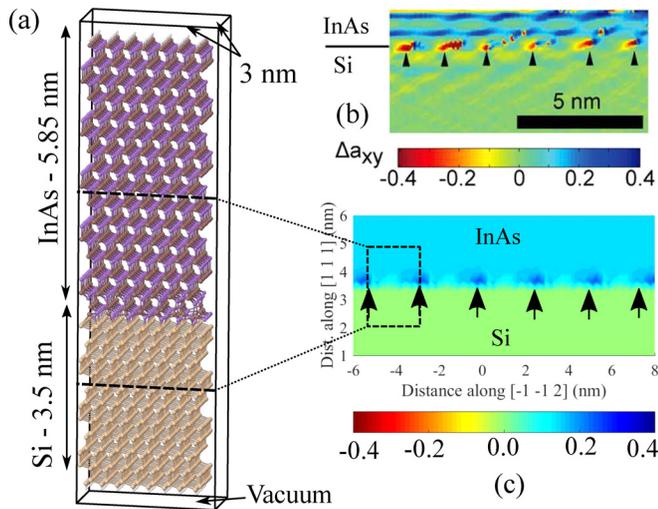


FIG. 2. (a) Unit cell of the InAs/Si slab used for electronic structure calculations. (b) The filtered TEM image of the InAs/Si interface showing the difference between the predicted lattice constant along [0 0 1] and the one obtained from the analysis of the TEM image. Reproduced with permission from Tomioka *et al.*, Nano Lett. 13, 5822 (2013). Copyright 2013 American Chemical Society. (c) Difference between the atomic position at the InAs/Si interface before and after geometric optimization projected along the [0 0 1] direction.

InAs/Si interface. Since both the Si and InAs layers in a TFET are very thick, i.e., bulk-like, an extremely thin slab such as the one used before cannot reliably represent the electronic states at the InAs/Si interface. On the other hand, DFT simulations of a bulk-like slab are computationally expensive. The InAs and Si layers in the slab are clipped to 16 bilayers and 11 bilayers, respectively. The geometrically optimized atomic structure of the InAs/Si interface obtained above is pasted at the interface of this clipped InAs/Si slab. The hexagonal supercell obtained this way is shown in Fig. 2(a) along with the cell boundaries. It is well known that the PBE pseudopotentials do not open a bandgap in bulk InAs and underestimate the gap in Si. Therefore, the pseudopotential developed by Tao *et al.* (Tao-Perdew-Staroverov-Scuseria-TPSS) is used.¹⁵ The scaling factor for exchange and the correlation part of the TPSS functional is set to 1.9 in order to reproduce the experimental value of the band gap in bulk InAs. Fermi-Dirac smearing is activated, and the temperature is set to 300 K. Initially, the energy minimization is performed with PBE pseudopotentials to obtain the total wave function of the structure. This wave function is taken as initial guess in the next step to perform the energy minimization using the TPSS technique.

The projection of the wave function of each energy level on spherical harmonics at each atomic position gives the atom-resolved density of states (DOS) of that energy level. The atom-resolved DOS of all the energy levels at each atom is temperature-broadened with a Gaussian broadening ($\sigma = 50$ meV) and summed up to compute the energy-dependent DOS on that atom. The atom-resolved DOS of all atoms in each monolayer in the (111) plane is averaged and plotted as a ribbon plot in Fig. 3 vs. energy. The ribbons are arranged in an increasing order of their distance from the bottom of the supercell. The valence band (VB) and the conduction band (CB) states separated by a bandgap of 1.1 eV

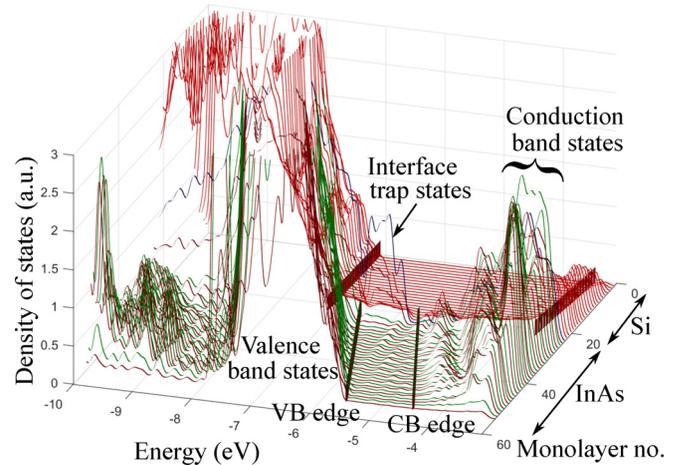


FIG. 3. Ribbon plot depicting the DOS in each monolayer of InAs and Si in the (111) plane. The DOS on In atoms is plotted in brown, on As atoms in green, and on Si atoms in red. The DOS of the As layer at the interface is plotted in blue to highlight the traps. The band edges are marked by the dark lines running across the slab.

are visible in the InAs slab. Similarly, CB and VB states are separated in the Si slab by a bandgap of 3.5 eV. The strong increase in the bandgap compared to the experimental bulk value is due to both quantum confinement in $\langle 111 \rangle$ and the use of the semi-empirical TPSS technique which overestimates the gap of Si. Also, the structure erroneously predicts type-I band alignment at the InAs/Si interface which may be attributed to the unequal shift of the VB edge due to confinement along $\langle 111 \rangle$ in the two slabs. The CB and the VB edges show a slope along $\langle 111 \rangle$ which is due to the residual electric field induced by the localized charges at the interface.

The DOS of As atoms at the InAs/Si interface is plotted as a blue ribbon in Fig. 3. It exhibits an unusual shape with a large DOS in the bandgap of InAs as compared to the Si or InAs ribbons in the bulk of the slab. This could be attributed to the trap energy levels at the interface. Among the adjacent monolayers of In, As, and Si at the interface, the As layer exhibits the highest DOS close to the VB edge, suggesting that the trap states are primarily located on the As atomic layer. The wave function of one representative trap level is shown as a contour plot in Fig. 4(b). It is highly localized on a labeled As atom at the interface. Additionally, the inspection of these atoms in Fig. 4 reveals that both atoms have one unsaturated orbital (dangling bond). Examination of the wave functions of other trap levels at the interface leads to the conclusion that all the trap levels are highly localized on one or a few As atoms at the interface. All the As atoms hosting the trap levels have at least one dangling bond. These atoms are colored in blue in Fig. 4(a) along with their labels. The above analysis suggests that the InAs/Si interface trap levels originate from dangling bonds present on As atoms at the interface.¹⁶

Interface traps must be passivated to minimize the trap-induced degradation of a heterojunction device such as a TFET. Since the interface traps originate from the unsaturated orbitals present on As atoms, hydrogen or sulfur atoms may be used to saturate the dangling bonds which will reduce D_{it} . The above developed atomistic model of the InAs/Si interface is used to study the effectiveness of

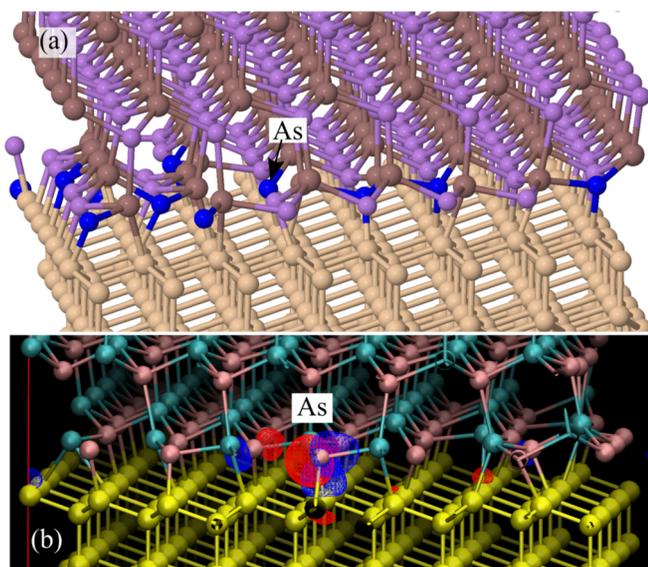


FIG. 4. (a) Atoms which contribute most to the trap levels are highlighted. All the As atoms hosting the trap levels have at least one dangling bond. (b) Contour plot of the wave functions of a representative trap level at $E = -6.253$ eV.

the two passivating materials. To study H passivation, hydrogen atoms are attached to the interface As atoms having unsaturated orbitals. Their exact position is determined by performing structural minimization of the InAs/Si slab by constraining all the atoms except the added H atoms. Electronic structural calculations of the converged structure are performed to obtain the ribbon plot (not shown) similar to that of Fig. 3. The atom-resolved DOS of the interface As atoms is found to be reduced after the passivation, implying the effectiveness of hydrogen passivation. The same study is performed by passivating the unsaturated interface As atoms by sulfur, except that the first two bi-layers of InAs are included in the structural minimization for determining the optimum position of the passivating S atoms. This is necessary since S atoms, due to a larger covalent radius, are expected to alter the atomic configuration in their vicinity.

The DOSs at interface As atoms with and without passivation are compared in Fig. 5. Passivation by both H and S significantly reduces D_{it} at the heterointerface. The VB DOS

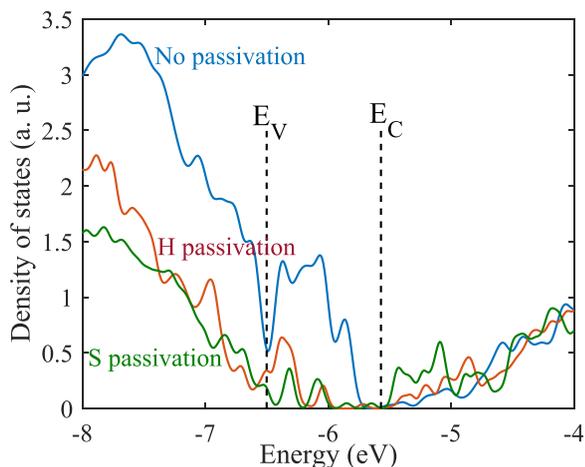


FIG. 5. Comparison of the density of states at the As monolayer at the interface with and without passivation.

at interface As atoms is large for the unpassivated interface compared to the passivated one. This is due to the trap states at the interface which capture/emit an electron and acquire a charge. This attracts electronic states in the VB towards the interface which, in turn, increases the atom-resolved DOS in the VB as seen in Fig. 5. When the traps are passivated, the local charge density at the interface is reduced which decreases the DOS at interface As atoms. The areal density of H or S atoms required for passivating the traps is close to 10^{14} atoms/cm². Introducing such a large number of H or S atoms at the interface *after* the growth is technologically challenging.

There are shortcomings and assumptions made in the above analysis. The lattice constants of Si and InAs in the analysis differ from their measured values. The use of experimental numbers would result in the relaxation of the interface during the structural minimization by high hydrostatic strain, not by the misalignment. To avoid it, the lattice constants of InAs and Si were relaxed beforehand. The bulk of InAs and Si slabs was assumed to be devoid of any defect during structural minimization of the interface. The growth of a polar semiconductor such as InAs on a nonpolar substrate such as Si may result in the formation of anti-phase domains. By tuning the growth conditions, an InAs nanowire can be grown from a single nucleation, and anti-phase domains can be avoided.

In conclusion, a reasonably reliable model of the atomic structure at the InAs/Si interface is obtained by structural minimization. The electronic structural calculations using this model reveal that the InAs/Si interface trap levels originate from unsaturated orbitals present on interface As atoms. The saturation of these unsaturated As atoms by H or S atoms is found to passivate the InAs/Si interface and to reduce D_{it} .

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