Integration of III-V heterostructure tunnel FETs on Si using Template Assisted Selective Epitaxy (TASE)

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Outline

- Motivation & background
  - Low power electronics
  - Tunnel FET functionality & SOA

- Template Assisted Selective Epitaxy
  - Vertical & Lateral approach

- Experimental
  - P & N-TFET fabrication
  - Electrical characterization

- Limitations of InAs/Si P-TFETs
  - Analysis of trap contributions

- Outlook & Summary
Low power electronics

\[ P_{tot} \approx C \cdot V_{dd}^2 \cdot f(V) + I_{\text{leak}} \cdot V_{dd} \]

Reduce \( I_{\text{leak}} \), Reduce \( V_{dd} \)

Steep subthreshold slope
\( \Rightarrow \) can decrease \( V_{th} \) to reduce \( V_{dd} \)
Tunnel FET functionality

- Steep slope $\Rightarrow V_{dd}$ scaling and low $I_{off}$
- Potential to achieve ultra-low power operation

Band-to-band-tunneling (BTBT) acts as bandpass filter cutting off the tails of the Fermi distribution
$\Rightarrow$ SS < 60 mV/dec possible
How to make a good tunnel switch

\[ I_{on} \sim T_{tunneling}^{WKB} = \exp \left( -\frac{4\lambda \sqrt{2m^* E_G^{3/2}}}{3qh(\Delta\Phi + E_G)} \right) \]

Increasing Ion

\( \lambda \): Electrostatics \( \rightarrow \) GAA, EOT scaling, thin body, doping profiles

\( E_g, m^* \): materials based \( \rightarrow \) Ge/InAs source on Si, III-V heterostructures

**GAA**

**Abrupt doping**

**High-k**

**III-V heterostructures**

- InAs
- Si
- GaSb
State of The Art Tunnel FETs

- Many different implementations (geometry, materials etc.) reported so far
- Varying potential for: High $I_{on}$, low $SS$, integration potential, scalability.

- InGaAs Air Bridge, Intel (IEDM 2011)
- s-SiNW on SOI (inverters), FZ Julich (IEDM 2013)
- InAs/GaSb mesa, Notre Dame (IEDM 2012)
- Planar Zn-diffused InGaAs, Tokyo University (IEDM 2013)
- GaSb/InAs vertical NW Lund (EDL 2016)
- Vertical Si-Ge NW, IMEC (IEDM 2013)
- 3D-2D TFET: MoS$_2$ & Ge, UCSB (Nature 2015)
Complementary TFET technologies

- Challenging for heterojunction TFETs, due to the need for different material combinations for n- and p-channel devices

- **VLSI 2015**: Demonstrated p- and n-type InGaAs/GaAsSb TFETs on the same InP substrate – use of metamorphic buffer

- Using TASE we are able to selective grow InAs and GaSb NWs co-planar to each other

- **VLSI 2016**: InAs/Si p-TFETs and InAs/GaSb n-TFETs are implemented on different wafers, using compatible process flows

- TASE technology for heterojunction TFETs
- Development of heterojunction TFET technology: vertical → planar
- Performance and limitations of fabricated TFETs


D. Cutaia et al., VLSI Symp. (2016)
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Vertical Implementation of TASE

Si/α-Si stack

α-Si

Si substrate

Etch sacrificial NW

Deposit SiO₂

Open template

α-Si selective wet etch

MOVPE growth

as-grown

Template stripped

III-V

GaAs

Applications: TFETs, dense integration, photovoltaics

- Large arrays possible → dense integration.
- Less flexibility in parameters, L & Lᵢ determined by stack.
Horizontal Implementation of TASE

- Good control over junction placement.
- Device parameters (L, L_i, W, etc.) easily defined by design.
- Easier fabrication

**Applications:** MOSFETs, TFETs, arbitrary geometry devices, optoelectronics
Template Assisted Selective Epitaxy (TASE)

Growth on any crystalline orientation

- Enables VLSI integration
- Requirement for Steep slope
- Scalable Technology

Stacked nanowires

Abrupt junctions

Chemical Analysis: EELS, EDX

Arbitrary geometries

- Courtesy of L. Gignac, IBM Yorktown.

Classical devices fabricated using TASE

InAs MOSFETs

Device:
10 parallel NWs, $L_G \sim 150$ nm,

Results:
- $I_{on} = 480 \mu A/\mu m$ ($V_{DS}=0.5V$)
- $g_m = 0.9$ mS/$\mu m$ ($V_{DS}=0.5V$)
- Field-effect mobility $\sim 500$ cm$^2$/Vs
- $SS = 250$ mV/dec

TASE grown Hall-bar structures

Hall measurements (0.1T, RT)
- $n_s = \frac{IB}{qV_H} = 3.9 \times 10^{17}$ cm$^3$
- electron mobility = 5400 cm$^2$/Vs

→ Material allows good device performance

H. Schmid et al. APL 2015,
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Developing our vertical InAs/Si TFET process

Transfer to lateral technology
flexibility in device processing & complementary TFETs
Horizontal TFET fabrication

1) P⁺ diffusion doping (PTFET)
2) Etch Si device layer
3) Oxide template & Si etch
Horizontal TFET fabrication

1) P⁺ diffusion doping (PTFET) 2) Etch Si device layer 3) Oxide template & Si etch

4) **PTFET:** InAs Source growth 4) **NTFET:** n-InAs(D)/InAs(C) & p-GaSb (S)

5) Template stripped
Horizontal TFET fabrication

1) P⁺ diffusion doping (PTFET) 2) Etch Si device layer 3) Oxide template & Si etch

4) PTFET: InAs Source growth

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6) Gate stack patterning
Horizontal TFET fabrication

1) $P^+$ diffusion doping (PTFET) 2) Etch Si device layer 3) Oxide template & Si etch

4) PTFET: InAs Source growth

4) NTFET: n-InAs(D)/InAs(C) & p-GaSb (S)

5) Template stripped

6) Gate stack patterning

7) S & D contacts
Horizontal InAs/Si p-TFETs

D. Cutaia et al., VLSI Symp 2016
Horizontal InAs/gaSb n-TFETs

D. Cutaia et al., VLSI Symp 2016
InAs/Si p-TFET: comparison vertical vs. planar

Observations:

- Ion boosted x50 by EOT scaling (vertical TFETs)
- Size: 100 nm cross-section → 30nm.
- Horizontal: \( SS_{ave} \) much improved 150 mV/dec → ~70mV/dec
Transfer Characteristics – 300K

- **P-TFET**: $I_{ON}=4\mu A/\mu m$ at $V_{GS}=V_{DS}=-0.5V$, $SS\sim 70-80mV/\text{dec}$, $I_{ON}/I_{OFF}\sim 10^6$
- **N-TFET**: $I_{ON}=40\mu A/\mu m$ at $V_{GS,ov}=3V$, $V_{DS}=0.5V$, $SS\sim 1V/\text{dec}$, $I_{ON}/I_{OFF}\sim 400$

Cutaia et al., VLSI Symp 2016
Transfer Characteristics – T-sweep

- Small T-dependence for $I_D$ in the ON state
- Strong SS T’dependence
  - **P-TFET**: $SS_{ave}$ reduced to 55mV/dec. at 150K
  - **N-TFET**: $SS_{ave}$ reduced to 400mV/dec. at 150K
SS and $g_m/I_D$ – p-TFET

Subthreshold Slope vs. $I_D$: Traps at InAs/Si heterojunction and InAs/High-k interface $\rightarrow$ Switching region limited by TAT

$g_m/I_D$ vs. $V_{GS}$: Transconductance efficiency peak at 300K $\rightarrow$ 34V$^{-1}$

Peak shifts to higher $I_D$ when reducing $T$ $\rightarrow$ SS improvement
Diode/Output characteristics

\[ V_{GS} = -1\text{V} \]
\[ V_{GS} = -0.5\text{V} \]
\[ V_{GS} = 0\text{V} \]
\[ V_{GS} = -0.5\text{V}, \text{no traps} \]

**P-TFET:** No NDR expected for \( V_{GS} \) levels used in measurements (-0.5V) due to gate overlap of source.

**N-TFET:** NDR observed on pn and pin diodes with gate metal removed, but not on TFETs

_S. Sant, submitted TED 2016_

_D. Cutaia et al., VLSI Symp 2016_
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Outlook & Summary
Effect of generation centers ("traps")

- Trap-assisted tunneling (TAT) can be seen as multi-phonon-assisted trap-band tunneling or as field-enhanced multi-phonon generation.
- Contribution from 3 kinds of traps: bulk, hetero interface, gate oxide interface

\[ \text{CB} \quad \text{VB} \]

traps at hetero interface

Bulk traps

oxide interface traps

\text{n-InAs} \quad \text{Silicon}

A. Palma et al., PRB 56, 9565 (1997)

F. Jiménez-Molinos et al., JAP, 91 (8), 5116 (2002)

\text{gate oxide}

\text{n-InAs}

\text{CB} \quad \text{VB}

A. Schenk et al. ULIS 2015, S. Sant et al., DRC 2016
Individual contributions of TAT mechanisms

- Only traps at InAs/Si hetero interface can give desired match with the experimental data

*S. Sant et al. submitted to IEEE TED*
Dominant mechanism - thermionic emission

- **Low gate bias**: thermionic emission is the bottleneck => SS close to thermionic SS.
- **Medium gate bias**: thermionic barrier is lowered => TAT becomes bottleneck.
- **High gate bias**: BTBT is dominating mechanism
Traps in InAs/Si TFETs

- Large lattice mismatch > 11% between Si and InAs.
- Predictive simulations show highest tolerable dit level ~ $5 \times 10^{11} \text{cm}^{-2}$.
- Extreme scaling required, or…..
- Use of lattice-matched material system $\rightarrow$ InGaAs/GaAsSb.
- Similar requirements on oxide $D_{it}$ levels.

One active trap level per dislocation $\rightarrow D_{it} = 1.5 \times 10^{13} \text{cm}^{-2}$

State-of-the-art TFETs

- Different designs $\rightarrow$ different merits
- $SS_{\text{ave}}$ scaling below 60 mV/dec in significant $I_{\text{on}}$ range still missing
Summary

- Introduced tunnel FETs and low-power electronics
- Demonstrated TASE growth for TFETs and device fabrication.
- Demonstrated scaled complementary TFETs
  – InAs/Si P-TFET & InAS/GaSb N-TFET
- Traps at the oxide and hetero interface are currently limiting performance.

Outlook

- Optimization of N-TFET (GaSb doping, gate stack)
- Reduction of defects → essential for all TFETs
- Applications of TASE to new fields: photonics, sensors,…
Thank you for your attention

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