Fabrication and electrical characterization of III-V heterostructure nanowire tunnel devices on silicon

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In this talk I will discuss our work on MOCVD growth of III-V nanowires (NWs) directly on a silicon substrate. The small dimensions of NWs relax the lattice matching requirements imposed by planar epitaxial growth, as the strain is relaxed through defect generation directly at the interface. This allows us, to investigate highly mismatched heterosystems, such as Si-InAs (11.6%).
We have investigated selective area non-catalyzed NW growth, and more recently we are focusing on growth within confined templates. The latter should allow us to tailor NW morphology more efficiently than when relying only on growth control.

In terms of devices, our main interest is on tunnel devices, Esaki diodes as well as tunnel FETs (TFET). In a TFET the effective tunneling bandgap determines the tunneling probability of charge carriers, hence the Ion. This makes the use of heterostructures particularly interesting, as it allows creating a small effective bandgap at the source heterojunction, while a larger bandgap material in the channel itself assures a high I_{on}/I_{off} ratio. Furthermore, the control of doping profiles is essential to achieve the desired device performance.
The reverse-bias current in an Esaki tunnel diode can be considered as the upper limit for the current output of a TFET. Recently, we demonstrated 6 MA/cm^2 in InAs-Si Esaki diodes, which is the 2nd highest reverse bias current ever reported in any III-V based system. For tunnel FETs the entire tunneling path is determining the device performance. It depends on device geometry, materials and the doping levels of the different sections. Thus the optimization to achieve combined high I_{on} and steep subthreshold slope continues.

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