Analysis of InAs-Si Heterojunction Double-Gate Tunnel FETs with Vertical Tunneling Paths

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***Abstract*—InAs-Si double-gate TFETs exploiting the two-dimensional (2D) density-of-state (DOS) switch are studied. A full-band and atomistic quantum transport simulator based on the $sp^3d^5s^*$ tight-binding model is used to solve the quantum transport problem taking into account both lateral and vertical band-to-band tunneling paths. TFETs with only vertical tunneling components are also investigated. Our findings suggest that InAs-Si 2D-2D TFETs might offer a device solution with both steep sub-thermal sub-threshold swing (SS) and high ON-current. In the best case of an extremely thin InAs-Si 2D-2D TFET the minimal swing reaches $SS = 12$ mV/dec and the ON-current 241 A/m.**

I. Introduction

Band-to-band tunneling (BTBT) FETs (TFETs) are being considered as the most promising candidates on the road towards energy-efficient transistors [1]. Among them, TFETs exploiting the "line tunneling" mechanism [2], [3], i.e. the vertical BTBT component with tunneling paths almost perpendicular to the gate, are expected to achieve much higher ON-currents than TFETs that use the so-called "point tunneling" mechanism, i.e. the source-channel lateral BTBT along the transport direction.

Line tunneling from quantized states in TFETs is an example for the matching of two density-of-states (DOSs) with different dimensionalities, the three-dimensional (3D) DOS of a bulk-like system and the two-dimensional (2D) DOS of the confined carrier gas at the semiconductor-oxide interface. TFETs featuring DOSs with reduced and/or different dimensionalities are summarized under the label *DOS switches*. Roughly speaking, a reduction of the dimensionality of the DOS will make it "sharper" and, therefore, will yield a steeper sub-threshold swing (SS). Other dimensionality combinations in TFETs are sparkign the interest of the device community. Recently, a new architecture known as Electron-Hole Bilayer TFET (EHBTEFT) [4] with vertical BTBT between a 2D electron gas and a 2D hole gas has been proposed. Although the idea of the EHBTFET is to enhance the BTBT current, so far, both experimental and numerical results agree upon a reduced ON-current [5] due to size- and bias-induced quantization. Indeed, a 1DEG and a 2DEG can only be formed by strong geometrical confinement which inevitably increases the band gap, i.e. the height of the tunnel barrier, with the consequences of a higher onset voltage and a reduced ON-current.

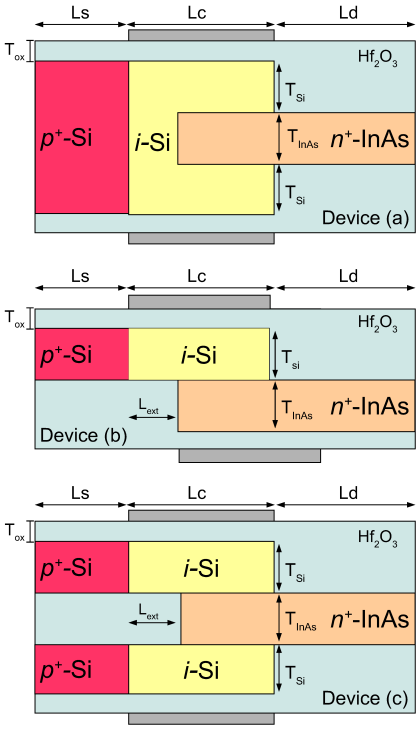

Fig. 1. Schematic view of the 2D-2D DOS switch TFETs studied in this work. $L_s = 20$ nm, $L_c = 30$ nm and $L_d = 20$ nm. The oxide thickness under the gate region is $T_{ox} = 1$ nm, whereas the doping concentrations for the source (n^+-type InAs region) and drain (p^+-type Si region) are $N_D = N_A = 5 \times 10^{19}$ cm^{-3}. For the devices (b) and (c) $L_{ext} = 10$ nm. The temperature in the devices is assumed to be 300 K.

InAs-Si [6]–[8] heterojunction TFETs have been identified over the last years as promising architectures to achieve respectable ON-current when comparing with conventional Metal-Oxide-Semiconductor FETs (MOSFETs). Combining heterostructures with 2D-2D DOS switches for TFETs (2D-2D TFETs) may lead to a

trade-off in the performance, i.e. in the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio. To maximize the performance, a high ON-current and a steep (sub-thermal) SS are required. In this work, the performance will be investigated for the InAs-Si 2D-2D TFETs shown in Figure 1. The full-band and atomistic quantum transport tool OMEN [9], which is based on a $sp^3d^5s^*$ tight-binding representation of the band structure, will be employed for the device simulations. 2D-2D TFETs based on metal-dichalcogenides (MoS_2 for the n-side and WTe_2 for the p-side) have already been investigated with OMEN [10]. Its multi-dimensional capabilities make it a suitable tool to analyze DOS switches taking into account the strong impact of quantization effects on the BTBT along all the possible paths.

II. InAs-Si 2D-2D TFET simulations

Figure 1 shows the design of InAs-Si heterojunction 2D-2D TFETs which are studied in this work: a 2D n^+-InAs quantum well (QW) (source) embedded (labeled as "device (a)") or laid on a 2D $\langle 111 \rangle$ Si QW (labeled as "devices (b)-(c)"). The gate length is 30 nm and the total device length is 65 nm. T_{InAs} and T_{Si} are the InAs and Si thicknesses, respectively. The doping concentrations are $N_{\mathrm{D}} = N_{\mathrm{A}} = 5 \times 10^{19}\,\mathrm{cm}^{-3}$, whereas the oxide thickness T_{ox} is set to 1 nm with an oxide permittivity $\varepsilon_{\mathrm{high}-\kappa} = 9$. Ballistic device simulations were performed with the TCAD tool OMEN and an in-house post-processing tool. A simplified metric has to be used: the values for SS are the minimal slopes and the ON-currents are the maximal currents found for a given source-drain bias. Note that only in semi-classical simulations the onset voltage can be determined by a threshold BTBT current which exceeds the Shockley-Read-Hall generation current of the reversed-biased diode. This allows for a proper averaging of SS over a few orders of magnitude in the current and a proper definition of the ON-current based on a given "overdrive" voltage. Here, as only ballistic BTBT currents are calculated, one has to use the (practically meaningless) point slope to compare the different structures and can only extract the "ON-current" at a particular V_{GS}.

Figure 2 shows the $I_{\mathrm{D}} - V_{\mathrm{GS}}$ transfer characteristics of device (a) with different thicknesses of InAs and Si. For the thinnest TFET, i.e. $T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 2\,\mathrm{nm}$, a very steep $SS = 12\,\mathrm{meV/dec}$ is found, while the ON-current at $V_{\mathrm{GS}} = -1.0\,\mathrm{V}$ has a value of 241 A/m. The thicker devices exhibit much higher ON-currents with the drawback of an increased SS. The maximum current they can reach is of the order of 10^3 A/m, while the SS is found to be 64 meV/dec for the device with

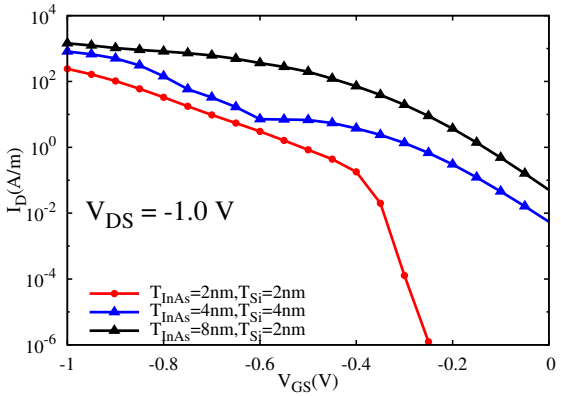

Fig. 2. Device (a): room-temperature $I_{\mathrm{D}} - V_{\mathrm{GS}}$ characteristics of InAs-Si 2D-2D p-TFETs with $V_{\mathrm{DS}} = -1.0\,\mathrm{V}$ computed with OMEN.

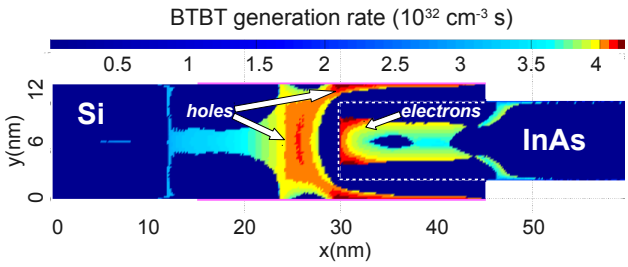

Fig. 3. Device (a): BTBT generation rate of an InAs-Si 2D-2D p-TFET with $T_{\mathrm{InAs}} = 8\,\mathrm{nm}$ and $T_{\mathrm{Si}} = 2\,\mathrm{nm}$ at $V_{\mathrm{GS}} = -0.2\,\mathrm{V}$ and $V_{\mathrm{DS}} = -1.0$ V. Here, in a post-processing step, the potential from OMEN has been used as an input.

$T_{\mathrm{InAs}} = T_{\mathrm{Si}} = 4\,\mathrm{nm}$ and 57 meV/dec for the device with $T_{\mathrm{InAs}} = 8\,\mathrm{nm}$ and $T_{\mathrm{Si}} = 2\,\mathrm{nm}$.

In order to better understand why the current within the sub-threshold regime is much higher in the case of the thicker devices, the BTBT generation rate at $V_{\mathrm{GS}} = -0.2\,\mathrm{V}$ is plotted in Figure 3. A non-local path BTBT approach has been implemented in an in-house tool with a Flietner imaginary dispersion [11], [12], as explained in the Appendix. The material parameters have been extracted from full band structures at the source and drain contacts computed with OMEN. For a Si QW with $T_{\mathrm{Si}} = 12\,\mathrm{nm}$ the effective mass and effective energy gap are: $m_{\mathrm{v}} = 0.147\,m_0$ and $E_{\mathrm{g}} = 1.34\,\mathrm{eV}$, respectively. For an InAs QW with $T_{\mathrm{InAs}} = 8\,\mathrm{nm}$ they are: $m_{\mathrm{v}} = 0.064\,m_0$, $m_{\mathrm{c}} = 0.04\,m_0$ and $E_{\mathrm{g}} = 0.58\,\mathrm{eV}$. In a post-processing step, the converged potential from OMEN is used as an input for the computation of the BTBT generation rate. As can be observed, both tunneling components (point and line tunneling) are present, the first one being the cause for the strong leakage current.

Devices (b) and (c) in Figure 1 are expected to show only line tunneling within the subthreshold regime since the lateral tunneling paths are truncated. However, for very low gate voltages, lateral intra-material tunneling

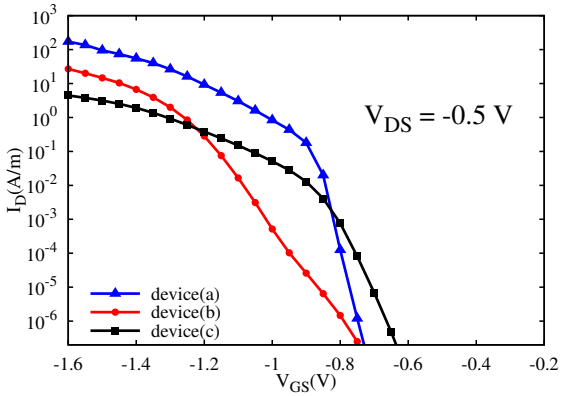

Fig. 4. Room-temperature $I_{\rm D}-V_{\rm GS}$ characteristics of InAs-Si 2D-2D p-TFETs, at $V_{\rm DS}=-0.5$ V for devices (a) (triangles), (b) (dots) and (c) (squares), computed with OMEN. The thicknesses are $T_{\rm InAs}=T_{\rm Si}=2$ nm in all cases.

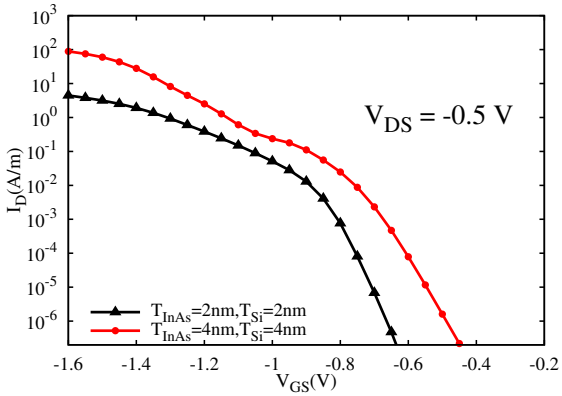

Fig. 5. Device (c): room-temperature $I_{\rm D}-V_{\rm GS}$ characteristics of InAs-Si 2D-2D p-TFETs, at $V_{\rm DS}=-0.5$ V for $T_{\rm InAs}=T_{\rm Si}=2$ nm (triangles) and $T_{\rm InAs}=T_{\rm Si}=4$ nm (dots), computed with OMEN.

may occur on the InAs side. Figure 4 compares the $I_{\rm D}-V_{\rm GS}$ characteristics of the three different InAs-Si 2D-2D p-TFETs with $T_{\rm InAs}=T_{\rm Si}=2$ nm in all cases and $V_{\rm DS}=-0.5$ V. As can be seen, device (a) still offers a better trade-off than its counterparts, with higher ON-current and very small SS. Device (b) gives a better ON-current than device (c), although the latter has a steeper SS. For the particular case of device (b) only intra-material tunneling was observed. Its hole and electron BTBT generation rates were located on the InAs side.

From the comparison of the $I_{\rm D}-V_{\rm GS}$ characteristics of device (a) and (c) in Figure 4 one can indirectly distinguish the impact and the contribution of point and line tunneling components. For instance, at the lowest gate voltages the difference between the currents is around two orders of magnitude. The current of device (a) is much higher due to lateral inter-material tunneling components, which are not present in device (c) when both InAs and Si layers are extremely thin, i.e. $T_{\rm InAs}=T_{\rm Si}=2$ nm. However, they have in common their steep slope as the result of the compromise between the effective gap $E_{\rm g}$ in InAs and the 2D-2D DOS switch. The larger the gap in InAs, the weaker the line tunneling that can contribute to the current, resulting in a smaller SS.

Figure 5 shows the $I_{\rm D}-V_{\rm GS}$ characteristics of device (c) for $T_{\rm InAs}=T_{\rm Si}=4$ nm and $T_{\rm InAs}=T_{\rm Si}=2$ nm. The strong confinement is reflected by the onset voltage. Also due to the lower energy gap, the thicker device presents a higher ON-current, but unlike device (a) the inter-material lateral leakage tunneling has vanished. As a consequence, the $SS=27$ mV/dec is comparable with its counterpart $SS=18$ mV/dec of the thinner device with the advantage of performing better (higher ON-current and lower onset voltage). This can be better observed in Figure 6 where the BTBT generation rate is plotted for the thicker device (c) at $V_{\rm GS}=-0.6$ V and $V_{\rm DS}=-0.5$ V. Here, only vertical tunneling takes place and no lateral tunneling component can be identified. Again, the Flietner imaginary dispersion was applied. Extracted from full band structures, the following parameters have been used: $m_{\rm v}=0.147\,m_0$ and $E_{\rm g}=1.34$ eV for Si, and $m_{\rm v}=0.0656\,m_0$, $m_{\rm c}=0.049\,m_0$ and $E_{\rm g}=0.68$ eV for InAs.

III. Conclusions

InAs-Si double-gate p-TFETs exploiting the 2D-2D DOS switch with different architectures have been simulated employing a full-band and atomistic quantum transport tool. Three device architectures labeled as device (a), (b), and (c) were studied. It was found that for the extremely thin versions of device (a), the $I_{\rm D}-V_{\rm GS}$ characteristics exhibit a very steep slope and a reasonably high ON-current. For extremely thin InAs-Si 2D-2D TFETs a swing of $SS=12$ mV/dec and an ON-current of 241 A/m were simulated. Thicker versions of it could provide much higher ON-current with the drawback of the deterioration of their corresponding SS. The latter

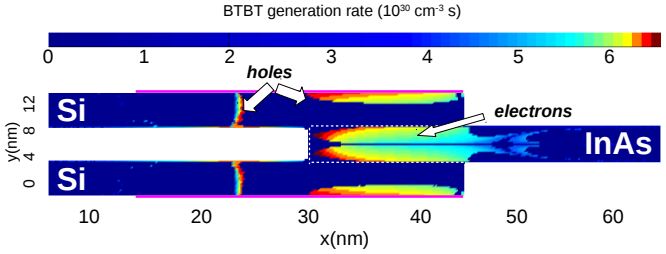

Fig. 6. Device (c): BTBT generation rate of a InAs-Si 2D-2D p-TFET with $T_{\rm InAs}=T_{\rm Si}=4$ nm at $V_{\rm GS}=-0.6$ V and $V_{\rm DS}=-0.5$ V. Here, in a post-processing step, the potential from OMEN has been used as an input.

is caused by the leakage current due to the lateral inter-material tunneling that is reduced in thinner devices by the larger energy gap.

Devices (b) and (c) were proposed in order to mitigate the leakage current. It was found that device (b) could perform better than device (c), although the latter gives a smaller SS. For an extremely thin device, (b), only intra-material tunneling on the InAs side was observed. The extremely thin device (c) presented the lowest ON-current, mainly due to the large energy gap in the extremely thin InAs layer that reduced the hole and electron generation rates. A thicker device (c) was also studied. Here, one could clearly observe that the lateral inter-material tunneling vanished, whereas the line tunneling, i.e. the vertical tunneling under the gate, was the only contribution to the current. Unlike device (a), the $I_{\rm D} - V_{\rm GS}$ characteristics still showed a steep slope comparable to its thinner counterpart with the advantage of having a much higher ON-current.

Although this study already reveals very important results for a better insight into 2D-2D DOS switches in InAs-Si double-gate TFETs, more material configurations, geometrical sizes, and device architectures have to be investigated. Work in this line is already in progress.

IV. Acknowledgment

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Appendix

Flietner Model and BTBT generation rate

Within 2-band analytical models, the Flietner model describes with high accuracy the imaginary band structure of materials with small band gap, such as the InAs, and it has the following form

$$\kappa = \sqrt{\frac{2m_{\rm c}E_{\rm g}}{\hbar^2}}\frac{\kappa_{\rm c}\kappa_{\rm v}}{\kappa_{\rm c}^2+(1-\alpha)\kappa_{\rm v}^2}, \tag{1}$$

where $m_{\rm v(c)}$ and $\kappa_{\rm v(c)} = \sqrt{2m_{\rm v(c)}|E-E_{\rm v(c)}|/\hbar^2}$ are the hole (electron) effective mass and the one-band imaginary dispersion for the valence (conduction) band, respectively. $E_{\rm g} = E_{\rm c} - E_{\rm v}$ is the energy gap and the parameter α is defined as $1-\sqrt{m_{\rm c}/m_{\rm v}}$. The Flietner model can be extended to the case of inter-material tunneling processes by treating the effective masses and energy gaps as position-dependent quantities [12], i.e. $m \to m(x,y)$ and $E_{\rm g} \to E_{\rm g}(x,y)$, respectively.

By replacing the energy variable (E) with the position based on the semi-classical expression of the BTBT current, $I_{\rm s-c} = q\int GdV$, and by using the Landauer formula, a relation between the generation rate G and the transmission probability $T_{\rm WKB} = \exp\left(-2\int_{r_{\rm v}}^{r_{\rm c}} {\rm d}r\kappa\right)$ can be established:

$$G_{\rm v(c),\mathbf{k}_\perp} = \frac{1}{\pi\hbar A}\sum_{\mathbf{k}_\perp} g_{\mathbf{k}_\perp}(U_{\rm v(c)})\nabla U_{\rm e} \tag{2}$$

$$g_{\mathbf{k}_\perp} = T_{\rm WKB}(\mathbf{k}_\perp, U_{\rm v(c)})\left\{f_{\rm L}(U_{\rm v(c)}) - f_{\rm R}(U_{\rm v(c)})\right\}, \tag{3}$$

with A being the cross section area perpendicular to the tunneling path direction, i.e. direction of the electric field. For a non-local path BTBT approach all possible trajectories starting at $r_{\rm v} = (x_{\rm v}, y_{\rm v})$ and ending at $r_{\rm c} = (x_{\rm c}, y_{\rm c})$ have to be taken into account.

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