InGaAs-on-Insulator FinFETs with Reduced Off-Current and Record Performance

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***Abstract*—**In this work, we demonstrate InGaAs-on-Insulator FinFETs on silicon with optimized on/off trade-off showing record performance. This is achieved by using carefully designed source/drain spacers and doped extensions to mitigate the off-current, typically high in narrow band-gap materials, as part of a CMOS compatible replacement-metal-gate process flow. Using this technology, devices with L_G = 20 nm, spacers width of 10 nm and W_{fin} = 15 nm achieve record high on-current of 350 µA/µm (I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), for scaled III-V FETs on Si, enabled by an access resistance of 220 Ω.µm, SS_{sat} = 78 mV/decade and g_m = 1.5 mS/µm. We analyze the impact of spacers thickness, W_{fin} and L_G on device performance. 2D TCAD simulations provide further insights into device functionality and about the dominant off-state leakage mechanisms.

I. Introduction

High electron mobility compound semiconductors such as InGaAs are considered promising candidates to replace Si as the channel material in nFETs in advanced CMOS nodes [1-3]. InGaAs can be integrated on silicon in a 2D co-planar [4] or 3D monolithic integration scheme [5], e.g. by use of direct wafer bonding [6], which can provide high-quality scaled III-V layers on silicon substrates, as well as incorporate a buried-oxide-layer (BOX) to enhance electrostatic confinement.

At scaled dimensions, 3D channel geometries such as fins or gate-all-around (GAA) nanowires are necessary to match the node target performances in terms of both electrostatics and current density. However, the floating body of such structures may lead to accumulation of holes in the channel region, triggering a parasitic bipolar transistor effect (PBE). This effect amplifies band-to-band tunneling (BTBT) current already significant in narrow band-gap materials, which further increases off-current (I_{OFF}) for InGaAs FinFETs [7]. The introduction of source-drain spacers have been suggested by simulations to reduce the effect of the PBE and to decrease I_{OFF} [8]. Previous works reporting the use of source/drain spacers show an off-current reduction [9-10] but also an increase of access resistance: optimized doped extensions beneath spacers are indeed necessary to limit this effect. So far, there has been no balanced implementation of sidewall spacers and low access resistance in III-V FETs.

In the present work, we experimentally investigate the reduction of I_{OFF} using spacers and source/drain doped extensions by fabricating and comparing $In_{0.53}Ga_{0.47}As$ FinFETs with several different spacer designs. As a result, we obtain devices with improved off-state performance, yielding a new on-current record at scaled L_G for III-V-on-Si.

II. Device Fabrication

The InGaAs FinFETs are fabricated using a III-V-on insulator platform on silicon substrates with a replacement-metal-gate (RMG) process and raised-source-drain (RSD) modules, as schematized in **Fig. 1**. The fabrication starts with the integration of a 20-nm thick $In_{0.53}Ga_{0.47}As$ channel layer on Si by using direct wafer bonding. Fins are patterned by HSQ (Hydrogen Silsesquioxane) resist and dry etched down to the BOX. Dummy high-k and dummy gate are deposited, patterned by HSQ and etched with an optimized inductively-coupled plasma reactive ion etching process (ICP-RIE). SiN_x is then deposited with variable thickness and spacers are formed on the dummy gate sidewalls by dry etching. The extensions and the RSD epitaxy are formed in one growth step by metalorganic chemical vapor deposition (MOCVD). The position of the extension is varied and adjusted with nm precision by performing several digital etching (DE) cycles prior to the growth. DE is done by using diluted HCl and ozone, resulting in an undercut underneath the spacers. Afterwards, an encapsulating inter-layer dielectric (ILD0) is deposited and planarized by chemical-mechanical polishing (CMP). This step enables access to the top of the dummy gate that is removed by a selective dry etch process. A scaled bilayer of Al_2O_3/HfO_2 high-k dielectric is deposited on the InGaAs channel by plasma-enhanced atomic-layer deposition (PE-ALD) followed by *in-situ* TiN metal gate deposition. Subsequently, the gate is filled with W which is planarized by CMP. A second oxide layer (ILD0') is deposited and finally, contact vias on source, drain and gate are opened and filled with W.

A high resolution cross-section TEM of an L_G = 20 nm device is shown in **Fig. 2a** and close-ups on the channel/contacts and channel/oxide interfaces are shown in **Fig. 2b,c**. In this work, we compare three different spacer designs, as shown in **Fig. 3**: without spacers as well as with 4 and 10 nm SiN_x spacers. A high-resolution fin TEM cross-section is shown in **Fig. 4**, showing excellent crystal quality as well as allowing for accurate measurement of fin dimensions.

III. Results and Discussion

First, we examine the influence of the S/D spacers on the off-current. **Fig. 5** shows I_{OFF}, defined as the minimum I_{DS}, versus gate length for FinFETs with W_{fin} = 25 nm, and with 0, 4 and 10 nm spacers. All data shown here are normalized to the gated periphery of the fins. At L_G = 100 nm, I_{OFF} is approximately one order of magnitude lower with 10 nm spacers compared to 4 nm spacers, and two orders of magnitude lower compared to no spacers. At L_G = 20 nm, this difference increases to three orders of magnitude.

Fig. 6 shows access resistance (R_{access}) versus spacer thickness. R_{access} = 220 Ω.µm is achieved for 10 nm spacers. Similar values of R_{access} are obtained for 4 nm (210 Ω.µm) and without spacers (200 Ω.µm), indicating that the doped extensions effectively mitigate increased R_{access} due to the ungated regions under the spacers, while still enhancing off-state performance. For devices with 10 nm spacers, the number of digital etches forming the RSD extensions was varied, resulting in 8 to 10 nm long extensions. R_{access} in turn varied by approximately 100 Ω.µm per nm of extension length below 10 nm, as shown in **Fig. 7**, which indicates the strong importance of a proper alignment of the doped extensions matching the width of the spacers. **Fig. 8** shows I_{ON}/I_{OFF} for the same devices. Here, I_{ON} is defined as I_{DS} at V_{GS} = $V_G(I_{OFF})$+1 V and V_{DS} = 0.5 V. 10 nm spacers improve I_{ON}/I_{OFF} by an order of magnitude compared to 4 nm spacers, indicating that I_{OFF} is reduced while maintaining I_{ON}.

To understand the influence of the spacers on the off-state performance and the origin of I_{OFF}, we perform 2D TCAD simulations of matching device structures using the same simulation set-up as in [8]. **Fig. 9** and **Fig. 10** show subthreshold characteristics of FinFET devices with W_{fin} = 30 nm and L_G = 300 and 100 nm respectively, all with 10 nm spacers. Experimental data (symbols) show a good match to simulated values (solid lines) in both on and off states for all gate lengths. Simulations indicate three sources of leakage currents in the off state [8]: (i) Trap-assisted tunneling (TAT) at the high-k/InGaAs interface on the drain side, (ii) source-to-drain tunneling (STDT), i.e. from the conduction band of the source to the drain, and (iii) BTBT, i.e. from the valence band of the channel to the drain. In addition, holes generated in the channel due to both BTBT and TAT lower the potential of the channel and increase the leakage through the forward-biased p-n junction on the source-side edge of the channel, which gives rise to the parasitic bipolar junction transistor effect (PBE) [11]. Since STDT is minimal in long-channel devices, due to the wide tunneling barrier, this effect of BTBT and TAT at gate-oxide/drain interface can be effectively suppressed by the 10 nm spacers utilized in this work. Note that traps may still be present at spacer/drain interface. Presence of a spacer eliminates formation of a triangular well at the interface, thereby inhibiting BTBT and TAT along the triangular well [8]. This eliminates major source of holes to the PBE and reduces off-state leakage. A similar effect is observed in the short channel devices as well. However, here the presence of STDT degrades the SS and slightly increases the off-state leakage.

Fig. 11 shows transfer characteristic of an L_G = 20 nm device, achieving I_{ON} = 350 µA/µm (I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), along with drain-induced barrier-lowering DIBL = 30 mV/V and subthreshold slopes in the linear and saturation regions, SS_{lin} = 74 and SS_{sat} = 78 mV/decade. The gate leakage (not shown) is lower than 1×10^{-10} A/µm. Peak transconductance reaches g_m = 1.5 mS/µm. **Fig. 12** shows output characteristics of the same device. Low output conductance is observed, as well as an on-resistance R_{ON} of 300 Ω.µm. $g_{m,peak}$ is shown versus L_G in **Fig. 13** for W_{fin} = 25 nm, exhibiting good scaling behavior and reaching 1.5 mS/µm at 20 nm, indicating strong resilience against short channel effects (SCEs). $g_{m,peak}$ is furthermore shown versus W_{fin} in **Fig. 14** for two gate lengths, 20 and 300 nm. At L_G = 300 nm, $g_{m,peak}$ remains approximately constant at 0.5 mS/µm, while at L_G = 20 nm, it scales with W_{fin}. Though increased surface scattering, reducing the electron mobility, is expected for scaled fins, the increase of $g_{m,peak}$ with W_{fin} can be explained by improved electrostatic control for narrow W_{fin}, which decreases g_d and improves extrinsic g_m. This is confirmed by **Fig. 15**, showing DIBL versus L_G for different W_{fin}, which strongly improves for narrow fins. **Fig. 16** and **17** show SS_{lin} and SS_{sat} versus L_G and W_{fin}, respectively. SS_{lin} reaches 65 mV/decade and SS_{sat} 78 mV/decade at L_G = 20 nm and W_{fin} = 15 nm. **Fig. 18** shows $I_{ON@IOFF,VDD}$, calculated at a fixed I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V, versus L_G for the three different spacer thickness. Even at fixed I_{OFF}, the reduced minimum I_{OFF} through the use of wide spacers enables higher I_{ON} due to a steeper SS near the I_{OFF} target. **Fig. 19** shows a benchmark of I_{ON} (at I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V) for various III-on-Si technologies [12-17]. Devices shown in this work achieve the highest reported I_{ON} = 350 µA/µm for III-V-on-Si FETs.

IV. Conclusion

We have demonstrated InGaAs FinFETs on silicon with optimized on/off trade-off showing record performance. This is achieved by using carefully designed source/drain spacers and doped extensions to mitigate the off-current. This enabled a reduction of the off-current by three orders of magnitude at scaled L_G, resulting in an improved SS_{sat} near the I_{OFF} target of 100 nA/µA while maintaining excellent R_{access}, leading to a record-high I_{ON} (V_{DD} = 0.5 V) of 350 µA/µm for III-V-on-Si FETs.

Acknowledgment

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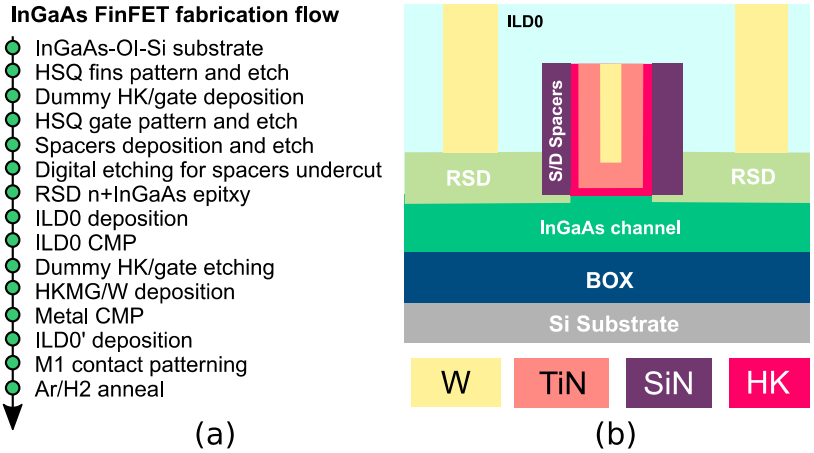

Fig. 1. (a) Process flow describing the self-aligned replacement-metal gate fabrication process for the InGaAs FinFETs presented in this work. (b) Schematic cross-section across the gate of the fabricated device. The InGaAs channel layer is 20 nm thick while the doped RSD InGaAs contacts are 25 nm thick. Doped extensions below the spacers are obtained by digital etching of the channel post-deposition of the spacers.

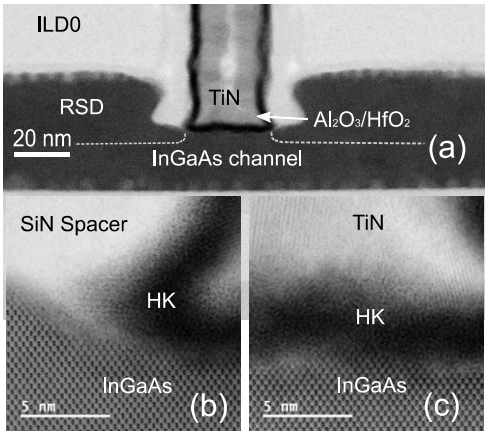

Fig. 2. (a) Cross-sectional STEM image of an InGaAs FinFET with L_G = 20 nm, showing SiN_x spacers and RSD contacts. (b) High resolution STEM close-up on the source side (c) and on the channel-HK interface.

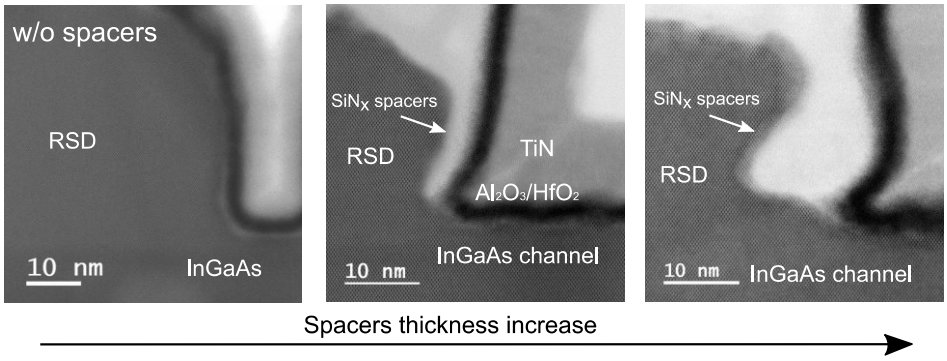

Fig. 3. Cross-sectional TEM images on the source-side gate region for the three spacer designs investigated in this work: (a) no spacers, (b) 4 nm spacers and (c) 10 nm spacers. The spacers are intended to reduce off-current leakage by reducing the parasitic bipolar effect through suppression of band-to-band tunneling as well as trap-assisted tunneling on the drain side.

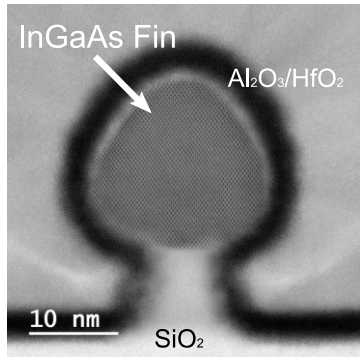

Fig. 4. STEM cross section of a fin with W_{FIN} = 20 nm. Excellent crystal quality is observed for the fin.

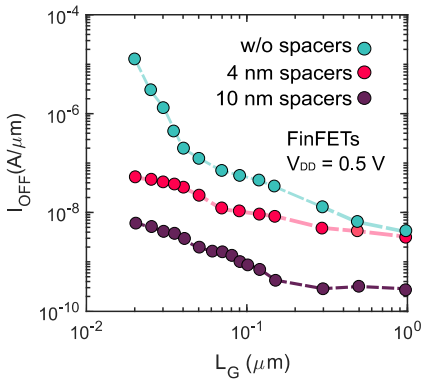

Fig. 5. I_{OFF} versus L_G. The I_{OFF} decreased by about 3 orders of magnitude at scaled L_G for devices with thicker spacers. The increase of I_{OFF} at smaller L_G is an indication of the presence of band-to-band tunneling and the resulting parasitic bipolar effect.

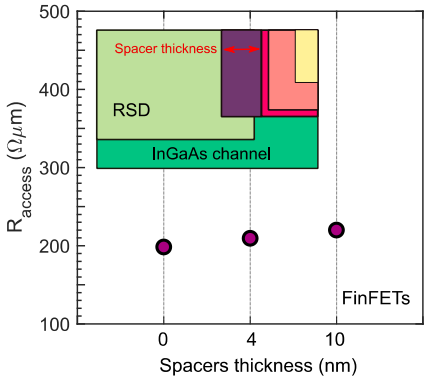

Fig. 6. Access resistance versus spacer thickness, as defined in the inset. The low R_{acc} value achieved for thick spacers devices indicates that the RSD spacer extensions effectively mitigate R_{acc} increase due to ungated regions under the spacers.

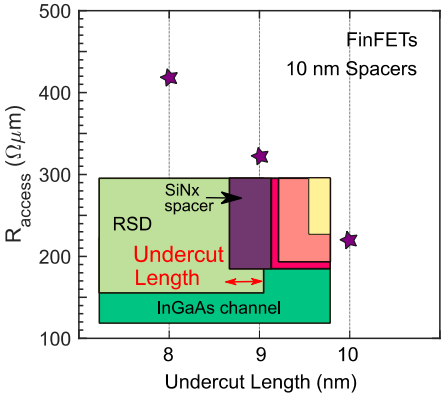

Fig. 7. Access resistance versus undercut length, as defined in the inset. The undercut length is set by the no. of digital etch cycles. This indicates the importance of carefully align the extensions region position to the sidewall spacers.

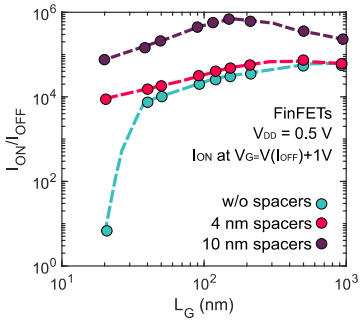

Fig. 8. I_{ON}/I_{OFF} versus L_G for FinFETs with and without spacers. The ratio is increased for shorter L_G. At long L_G, the higher I_{OFF} is balanced by the higher I_{ON} for the devices without spacers.

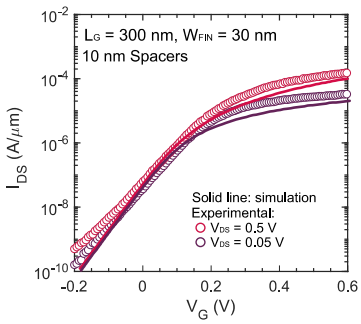

Fig. 9. Subthreshold characteristics of FinFET device with 10 nm spacers, W_{fin} = 30 nm and L_G = 300 nm. Solid traces show 2D TCAD simulations, that show excellent fit of experimental data (symbols).

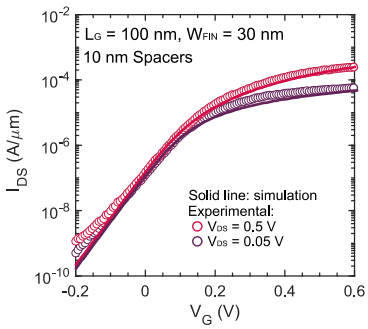

Fig. 10. Subthreshold characteristics of FinFET device with 10 nm spacers, W_{fin} = 30 nm and L_G = 100 nm. Solid traces show 2D TCAD simulations, that show excellent fit of experimental data (symbols).

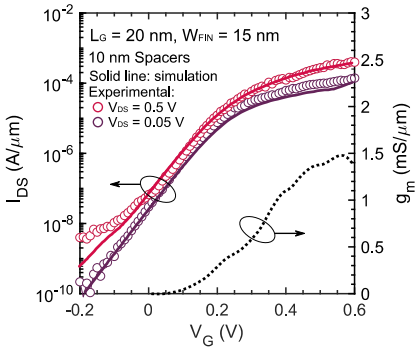

Fig. 11. I_D/V_G of FinFET device with 10 nm spacers, W_{fin} = 30 nm and L_G = 20 nm. This device exhibits record high I_{ON} of 350 μA/μm (at I_{OFF} = 100 nA/μm, V_{DD} = 0.5 V).

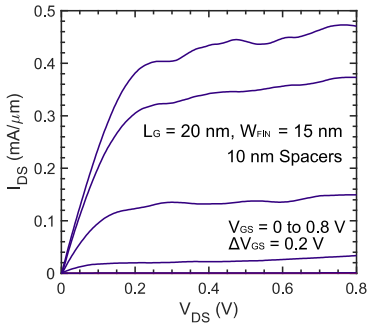

Fig. 12. Output characteristic of a L_G = 20 nm device with W_{FIN} = 15 nm. Low g_d is observed, along with R_{ON} = 300 Ω.μm.

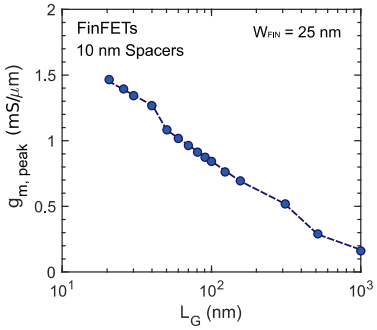

Fig. 13. Peak g_m versus L_G for FinFETs with 10 nm spacers, showing excellent scaling behavior down to L_G = 20 nm.

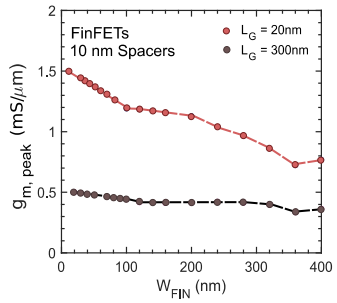

Fig. 14. Peak g_m versus W_{fin} for long and short channel devices. g_m increases in the latter due to reduction of g_d.

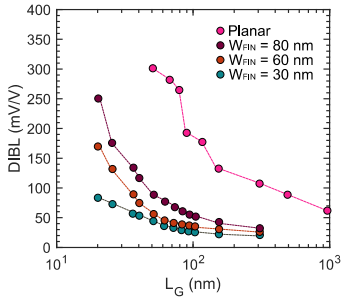

Fig. 15. DIBL vs L_G for different channel designs, showing strongly improved electrostatic control for narrow fins.

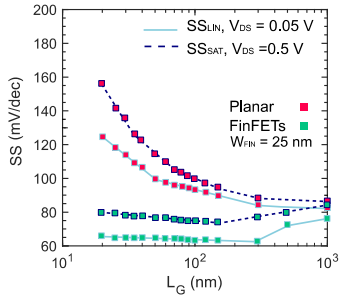

Fig. 16. Minimum SS in saturation and linear regime versus L_G for both planar and FinFET devices.

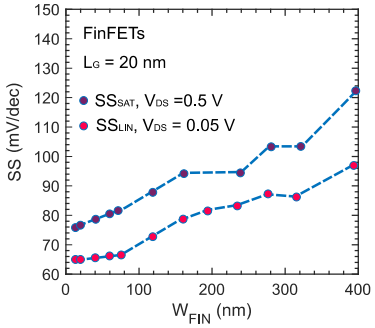

Fig. 17. Minimum SS in saturation and linear regime versus W_{fin} at L_G = 20 nm, showing the importance of fin width scaling. At minimum W_{fin}, SS_{sat} = 78 mV/decade is achieved.

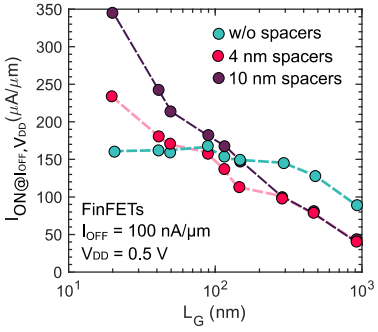

Fig. 18. On current versus gate length for III-V FinFETs devices with three different spacer designs. The presence of spacers generally improves I_{ON} at scaled L_G because of the lower SS close to the target I_{OFF} = 100

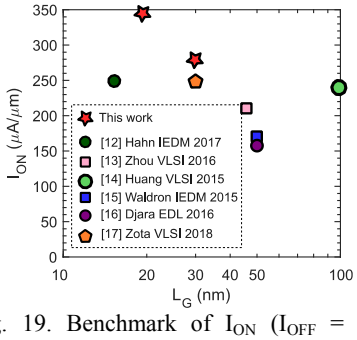

Fig. 19. Benchmark of I_{ON} (I_{OFF} = 100 nA/μm, V_{DD} = 0.5 V) versus L_G for different III-V-on-Si technologies. The value of 350 μA/μm shown in this work represents the highest reported for this type of device.