

The Impact of Hetero-junction and Oxide-interface Traps on the Performance of InAs/Si Tunnel FETs

Andreas Schenk¹, Saurabh Sant¹, Kirsten Moselund², and Heike Riel²

¹Integrated Systems Laboratory, ETH Zurich, CH-8092 Zürich, Switzerland, schenk@iis.ee.ethz.ch

²IBM Research-Zurich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland

Abstract

The effect of traps in the hetero-junction and at the oxide interface on slope and ON-current of vertical and lateral InAs/Si Nanowire (NW) Tunnel FETs (TFETs) is demonstrated through physics-based TCAD analyses in combination with experimental findings. The high density of interface states (D_{it}) at the highly lattice-mismatched material interface degrades the sub-threshold swing (SS) and makes band-to-band tunneling (BTBT) completely dominated by Shockley-Read-Hall (SRH) generation and trap-assisted tunneling (TAT) up to high gate voltages. When the NW diameter is scaled into the volume-inversion regime, the TFET can even turn into an artificial MOSFET with close-to-60mV/dec slope due to the intrinsic Si channel. The only remedy is then given by a “trap-tolerant” geometry where the gate edge is aligned with the hetero-junction.

(Keywords: Tunnel FETs, steep slope, trap-assisted tunneling)

Introduction

TAT via interface and bulk traps is the main non-ideality effect in TFETs, besides channel quantization, surface roughness, and density-of-state (DOS) tails [1]. SS and ON-current are influenced by physical parameters like D_{it} , capture cross sections, relaxation energies, roughness amplitude, and width of the DOS tail. Temperature-dependent IV -measurements are mandatory to assess the contributions of SRH and TAT generation. Two kinds of InAs/Si NW hetero TFETs were fabricated by template-assisted selective epitaxy and electrically characterized: vertical (Fig. 1) with diameter ~ 100 nm [2] and lateral (Fig. 4) with diameters down to ~ 30 nm [3]. Simulations with a set-up described in [4,5] yielded good agreement with the measured temperature-dependent transfer characteristics.

Simulation set-up

In the present TCAD study, BTBT is modeled by the so-called *dynamic nonlocal path model* [6] with band structure parameters listed in the caption of Fig. 1. The nonlocal TAT model in [6] is based on Ref. [7]. These models and parameters, which are also used here, provided good agreement with measured

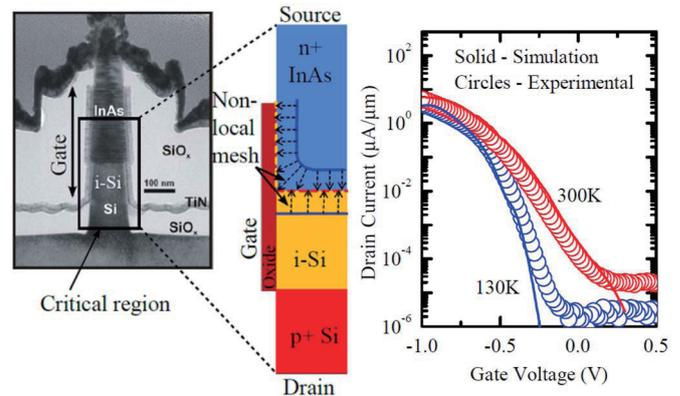


Fig. 1: (left) TEM image of the InAs/Si vertical NW TFET (taken from [2]). (middle) Radial cross section of the critical region in simulation. (right) Comparison of exp. and sim. transfer characteristics [4]. Parameters for InAs: $E_g = 0.36$ eV, $m_c = 0.023 m_0$, $m_{lh} = 0.026 m_0$; for Silicon: $E_g = 1.11$ eV, $m_c = 0.19 m_0$, $m_{lh} = 0.15 m_0$; valence band offset = 130 meV.

I_D - V_{GS} curves of the lateral nanowires [5] shown in Fig. 4. Traps at the InAs/oxide interface are assumed to be uniformly distributed in the band gap with $D_{it} = 1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ found experimentally in Ref. [8]. At the InAs/Si interface the energetic trap distribution was assumed to be Gaussian with its peak at the valence band (VB) edge, a peak $D_{it} = 1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, and a full-width half maximum of 220 meV.

Trap-assisted tunneling in InAs/Si pTFETs

Fig. 2 compares the ideal BTBT current (solid blue curve) with TAT currents due to bulk traps in the InAs-Si hetero junction of the vertical NW TFETs of Fig. 1. No value of the lattice relaxation energy can

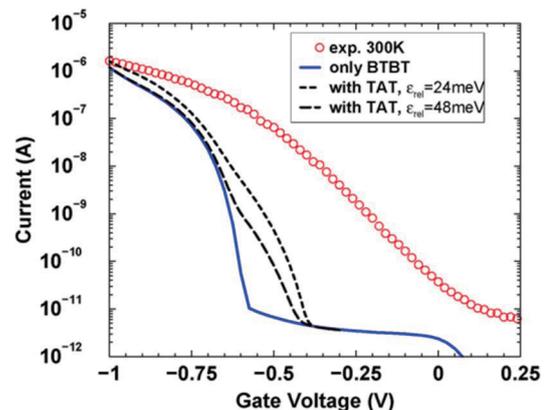


Fig. 2: Simulated TAT currents at 300 K due to bulk traps in the InAs-Si hetero junction for different values of the lattice relaxation energy (broken lines).

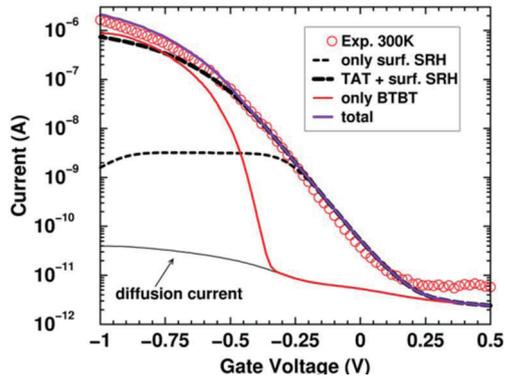


Fig. 3: Current contributions at 300 K due to traps at the InAs/oxide interface. Parameters: $D_{it} = 1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, $V_{\text{trap}} = 10 \text{ \AA}^3$, $\sigma_n = \sigma_p = 1 \times 10^{-14} \text{ cm}^2$.

explain the strong leakage current and the weak slope measured at 300 K. By assuming traps at the InAs/oxide interface *only*, one obtains a perfect fit of the measured current at 300 K as shown in Fig. 3. A deeper inspection reveals the individual contributions to the total current: In the lowest branch it is determined by surface SRH generation, which reaches a plateau at $V_{\text{GS}} = -0.25 \text{ V}$ where TAT starts to dominate. Only at -1 V the current is due to BTBT. At 130 K the same parameters (shown in the caption of Fig. 3) result in a complete underestimation of the current. As the TAT process is found to be zero-phonon, only capture coefficients which increase with decreasing temperature would explain this behavior. Thus one can conclude that at low temperatures traps at the hetero-interface become dominant. Including them gives a good fit for both temperatures as shown in Fig. 1.

A different behavior is found in the lateral devices shown in Fig. 4. Due to the small diameter, surface inversion cannot take place which inhibits TAT at the oxide interface. The TAT current is generated by

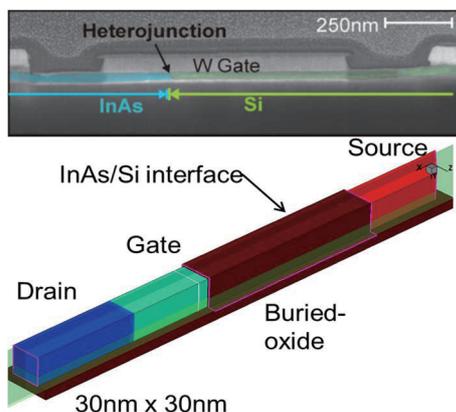


Fig. 4: (top) SEM image of the lateral InAs/Si NW TFET with inclined hetero-interface (taken from [3]), (bottom) 3D simulation domain.

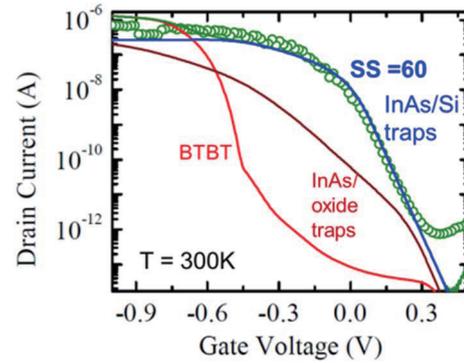


Fig. 5: Individual contributions of BTBT and TAT processes to the transfer characteristics of the lateral InAs/Si NW TFET (Fig. 4) at 300 K. Solid lines: simulation, circles: measurement.

hetero-interface traps; oxide-interface traps only change the electrostatics when occupied. The simulated current shown in Fig. 5 fits well the experimental curve at 300 K with a swing of $\sim 60 \text{ mV/dec}$ [2]. The band diagram in Fig. 6 makes clear that the strong TAT generation at the hetero-interface plays the role of a current source in an internal MOSFET. The latter is electrostatically formed as the charged interface states together with the gate voltage create a thermionic barrier to the flow of holes towards the drain contact. The gate control of the artificial MOSFET is almost ideal due to the intrinsic Si channel which explains the measured slope close to 60 mV/dec. The comparison in Fig. 7 shows three distinct segments of the transfer curve - thermionic emission, TAT, and BTBT - being the bottleneck at low, intermediate, and high V_{GS} , respectively. Assuming the same D_{it} for all kinds of traps, it turns out that $D_{it} < 5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at both interfaces is required to reach sub-thermal SS which, however, is still caused by TAT [5].

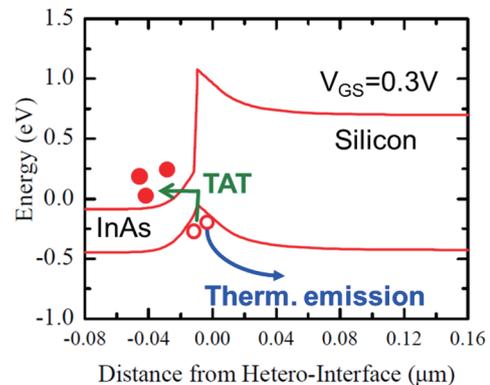


Fig. 6: Band diagram along the channel at the onset of the TFET. Due to the high defect density at the InAs/Si interface, transport of carriers happens via two subsequent steps, viz., TAT generation of e-h pairs and thermionic emission of holes.

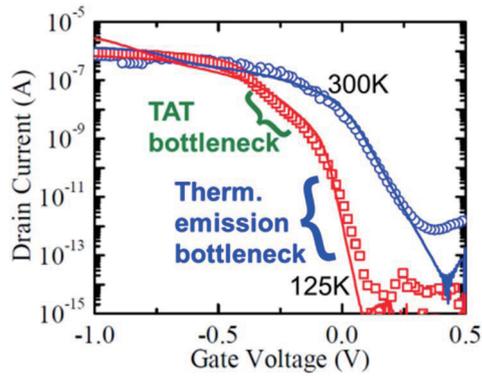


Fig. 7: Transfer characteristics at two different temperatures reveal three distinct intervals of the transfer curve, where the current originates from thermionic emission, TAT, or BTBT, respectively.

Trap-tolerant device geometry

Although diameter scaling suppresses TAT at the oxide interface, TAT at the InAs/Si hetero-junction remains a leakage source at the onset of BTBT in the NW pTFET, which is detrimental to low-power application. A reduction of the D_{it} at the hetero interface is possible with lattice-matched material systems [9]. Nevertheless, the question arises whether despite a high defect concentration the onset of BTBT can be accelerated by geometry changes such that it obscures TAT. One possibility is the alignment of the gate edge with the InAs/Si

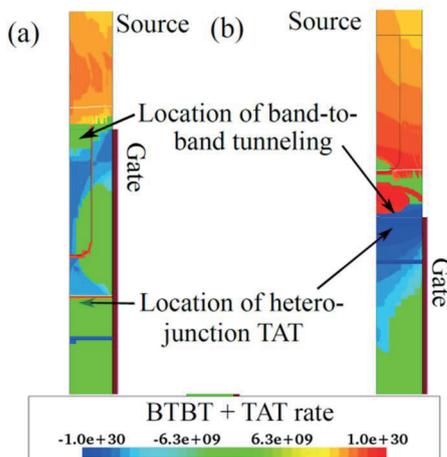


Fig. 8: BTBT and TAT rates along the radial cross section of an InAs/Si NW pTFET ($d = 20$ nm) with (a) gate-overlapped-source (GOS) and (b) gate-aligned (GA) geometries.

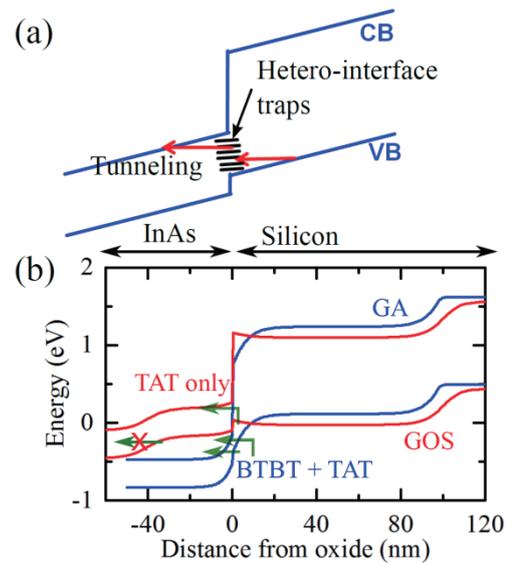


Fig. 9: (a) Schematic diagram showing TAT at the hetero-interface. (b) Extracted band edge diagrams along the axis of the TFETs at $V_{GS} = -0.5$ V.

hetero-interface. Simulation results for a NW TFET ($d = 20$ nm) with gate alignment (GA) and with gate-overlapped-source geometry (GOS) are compared in Fig. 8. The gate alignment has the effect that BTBT occurs at the same location and starts at the same voltage as TAT. As seen from the band edge diagram (Fig. 9) extracted along the axis of the two TFETs at the onset of tunneling ($V_{GS} = -0.5$ V), both BTBT and TAT have already started in the GA TFET. On the contrary, only TAT has begun at the hetero-interface in the GOS TFET while BTBT is yet to begin. The simultaneous onset of TAT and BTBT in GA TFETs not only improves the SS but also results in a lower leakage floor. This is seen in Fig. 10 which presents transfer characteristics of the GOS TFETs with large and small diameter, respectively, the GA TFET with small diameter, and the measured curve at 300 K from Fig. 1 (c) for comparison. Diameter scaling alone results in a steep branch (although not sub-threshold), but also in a high leakage floor and a strongly reduced ON-current. The GA geometry removes the leakage floor and nearly recovers the ON-current. The steep branch becomes extended and slightly sub-threshold.

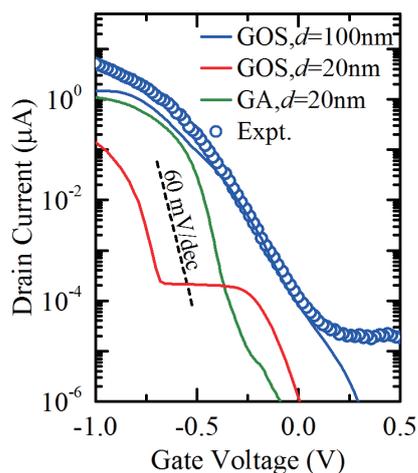


Fig. 10: Simulated transfer characteristics of the GOS and GA TFETs at 300 K. Experimental data of Fig. 1 (c) are shown for comparison.

Conclusion

Low defect densities at interfaces are needed to achieve sub-thermal slope in InAs/Si NW TFETs. By combining defect characterization, temperature-dependent IV -measurements, and physics-based TCAD simulations one can estimate an upper limit for the D_{it} of $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Scaling the diameter into the volume-inversion regime suppresses TAT at the oxide interface, but increases the leakage current floor and reduces the ON-current. Alignment of the gate edge with the hetero-junction accelerates BTBT and results in an extended branch with sub-thermal slope. The value of the ON-current is nearly the original one. The suggested methods to improve the tolerance of hetero TFETs against interface traps are accompanied by some drawbacks. Diameter scaling can not only increase the tunnel barrier as consequence of size quantization but also make the transistor susceptible to the electrostatic effect of single charges at the oxide interface or in the oxide if they are located close to the point of maximum tunnel generation. In a GA TFET, a misalignment of 1-2 nanometers between gate edge and hetero-interface can notably alter the slope. These deviations can cause large performance fluctuations from sample to sample and, therefore, call for further investigations.

Acknowledgments

Funding from the European Community's Seventh

Frame-work Program under Grant Agreement No. 619509 (Project E2SWITCH) is acknowledged.

References

- [1] A. Schenk, S. Sant, K. Moselund, and H. Riel, "III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects" Proc. EUROSIOI-ULIS, Jan 25-27, 2016, pp. 9-12, doi: 10.1109/ULIS.2016.7440039
- [2] D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, and H. Riel, "Complementary III-V heterojunction lateral NW tunnel FET technology on Si," Symp. VLSI Technol., p. 21.3, 2016.
- [3] K. E. Moselund, D. Cutaia, H. Schmid, M. Borg, S. Sant, A. Schenk, and H. Riel, "Lateral InAs/Si p-Type Tunnel FETs Integrated on Si - Part 1: Experimental Devices", IEEE Trans. Electron Devices, Vol. **63** (11), 4233, Nov. 2016.
- [4] S. Sant, A. Schenk, K. Moselund, and H. Riel, "Impact of Trap-assisted Tunneling and Channel Quantization on InAs/Si Hetero Tunnel FETs", IEEE 74th DRC, p.67, 2016.
- [5] S. Sant, K. E. Moselund, D. Cutaia, H. Schmid, M. Borg, H. Riel, and A. Schenk, "Lateral InAs/Si p-Type Tunnel FETs Integrated on Si - Part 2: Simulation Study of the Impact of Interface Traps", IEEE Trans. Electron Devices, Vol. **63** (11), 4240, Nov. 2016.
- [6] Sentaurus-Device User Guide, Version 2015.06, Synopsys Inc., Mountain View, CA, USA, 2015.
- [7] A. Palma, A. Godoy, J. A. Jimenez-Tejada, J. E. Carceller, and J. A. Lopez-Villanueva, "Quantum two-dimensional calculation of time constants of random telegraph signals in metal-oxide – semiconductor structures", Phys. Rev. **B 56**, 9565 (1997).
- [8] P. Mensch, K. E. Moselund, S. Karg, E. Lörtscher, M. T. Björk, and H. Riel, "Interface State Density of Single Vertical Nanowire MOS Capacitors", IEEE Trans. Nanotechnology **12**, 279, 2013.
- [9] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb Tunneling Field-Effect Transistor on Si with $S = 48 \text{ mV/decade}$ and $I_{on} = 10 \mu\text{A}/\mu\text{m}$ for $I_{off} = 1 \text{ nA}/\mu\text{m}$ at $V_{DS} = 0.3 \text{ V}$ ", IEDM Tech. Digest, p. 500, Dec. 2016.