Analysis of Cooling-induced Strain in 5-Gate FinFETs and its Impact on Hole Qubits

Participating research groups: Nano-TCAD Group, ETH Zurich

Authors: Andreas Schenk, Qian Ding, and Mathieu Luisier

Abstract - We performed TCAD simulations of cooling-induced strain and its impact on the electrostatics in 5-gate hole spin qubit Si FinFET fabricated at the University of Basel. Stress and strain distributions after cooling from 300 K to 1 K were obtained with an experimental mechanics simulator of Synopsys. We studied how the strain changes when TiN gates are replaced by poly-silicon gates. Two methods of strain calculation and three different boundary conditions were compared. The impact on electrostatics and hole localization was simulated with Sentaurus-Device based on the 6x6 k·p theory (Bir-Pikus model) and the density-gradient method to mimic the 3D confinement of single holes under the plunger gates. Albeit the cooling-induced strain and its longitudinal gradients are non-negligible, they cannot explain hole localization under experimental bias conditions.

Device Structure & Strain Simulation Methods

Device Structure:

- We studied the 5-gate Si FinFET fabricated at Uni Basel [1] (Fig.1a) using the 3D device structure shown in Fig.1b for strain (Fig.1c) and electrostatics TCAD simulations.
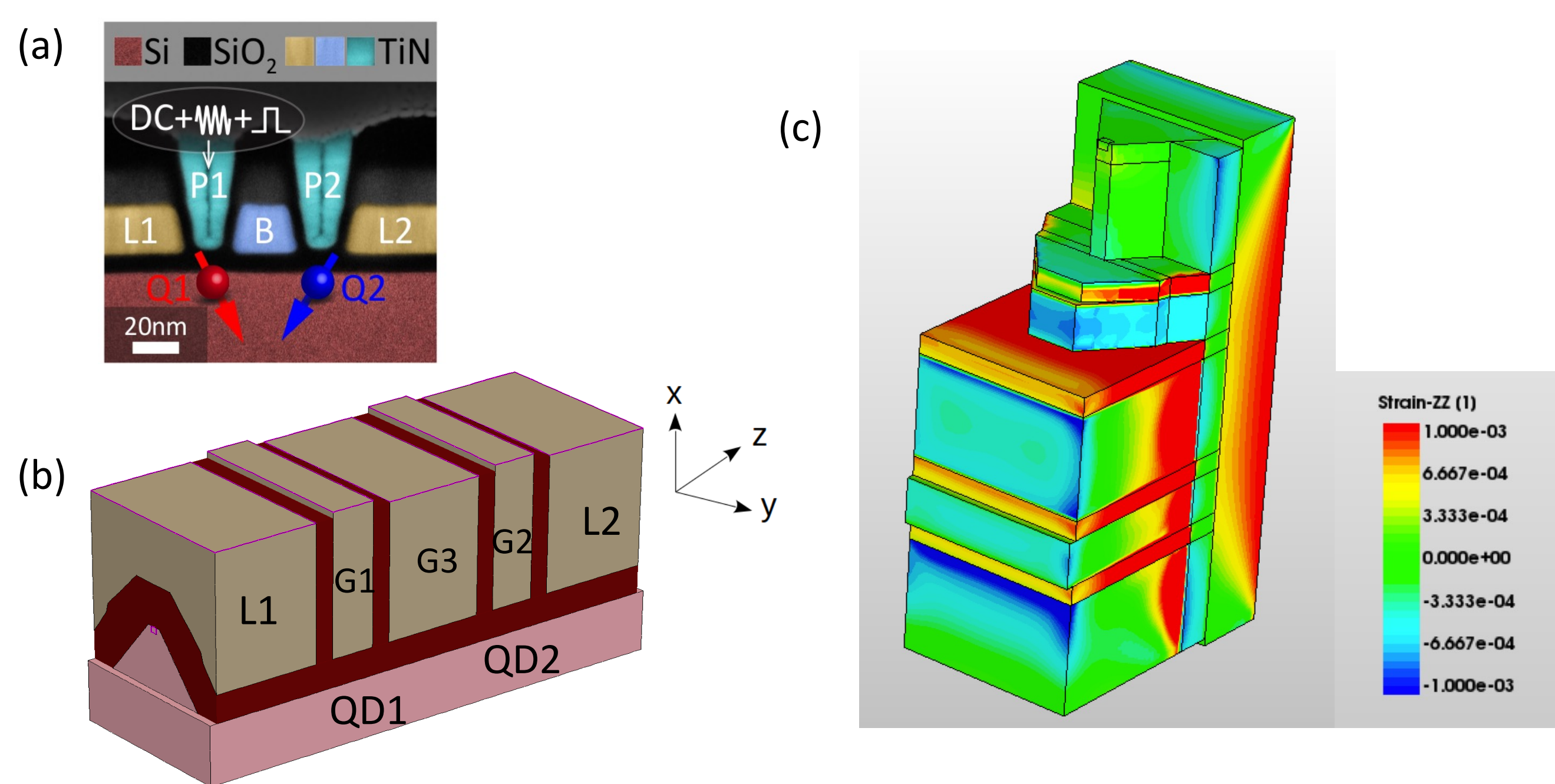

Figure 1: (a) 2D cross section of fabricated 5-gate Si FinFET device along fin direction, with double QDs formed under P-gates. (b) Sketch of simulated 3D device structure. (c) zz-component of strain tensor after cooling from 300 K to 1K.

Simulation Methods:
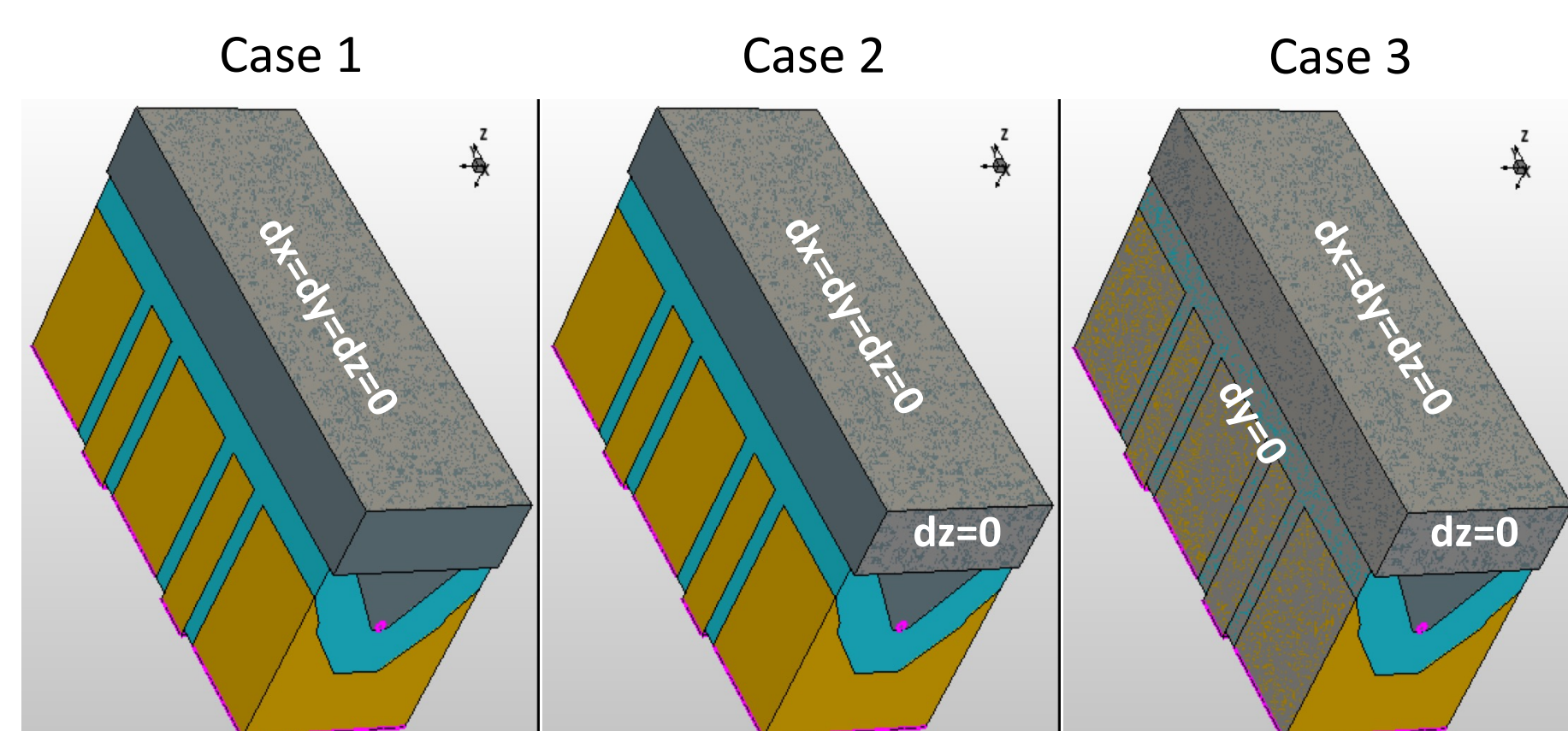
- Test of different boundary conditions:

Figure 2: Three cases of boundary conditions (BCs): (left) Zero Dirichlet in all directions on ground plane. (middle) Zero Dirichlet in all directions on ground plane and in z-direction on side planes of substrate. (right)) Zero Dirichlet in all directions on ground plane, in z-direction on side planes of substrate, and in y-direction on all y-side planes. Free-moving BCs elsewhere.

- Two methods of strain simulation result in different profiles as illustrated in Fig. 3:
    1) Strain simulated in linear elastic model as symmetrised gradient tensor of the total displacement field; then imported in S-Device for electrostatics simulation.
    2) Stress from Synopsys mechanics simulator used to compute strain in S-Device as compliance tensor *times* stress, followed by electrostatics simulation [2].
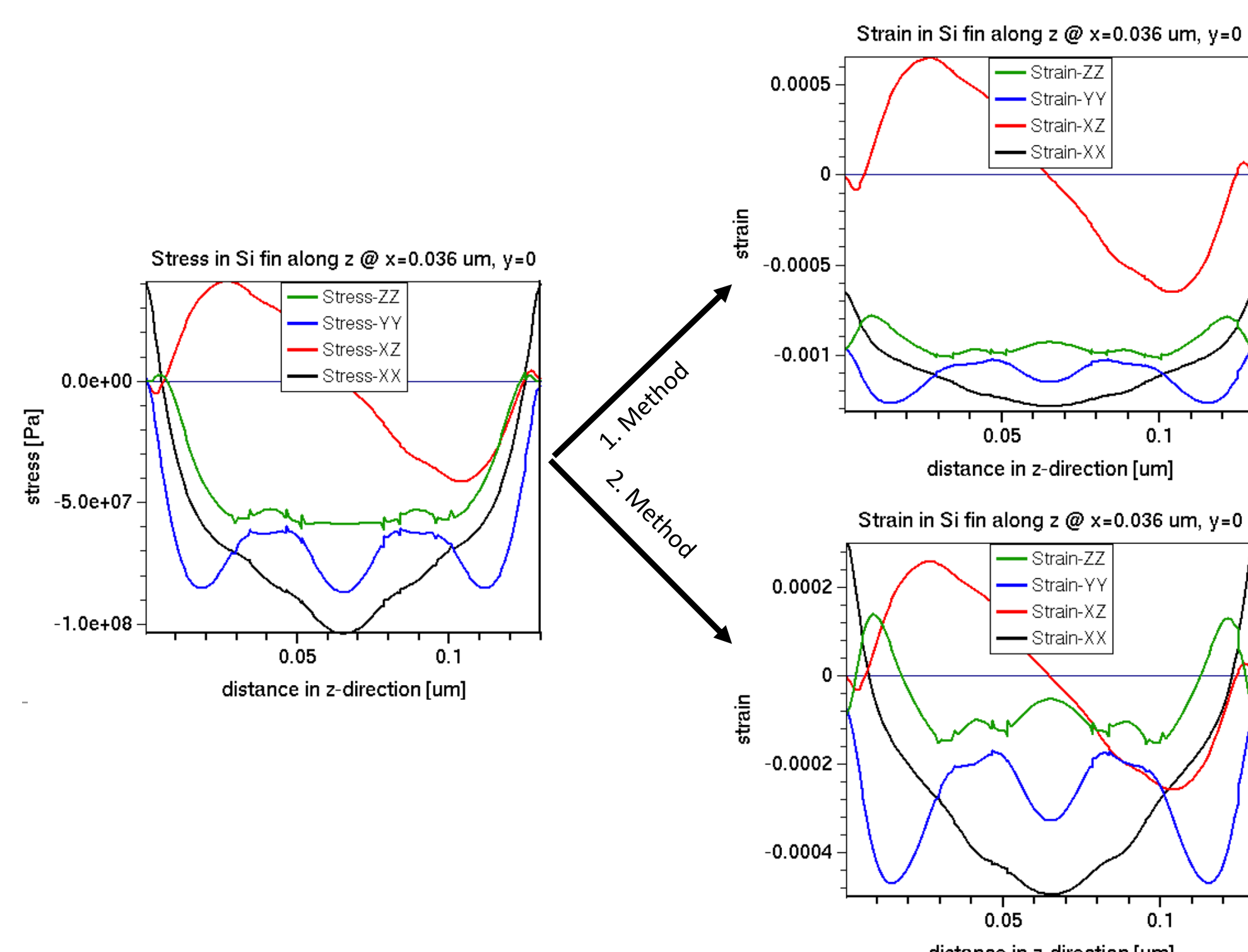

Figure 3: Simulation methods for the cooling-induced strain. The first method covers the strain due to free expansion (contraction), the second method only the stress-related strain. BC Case1 shown.

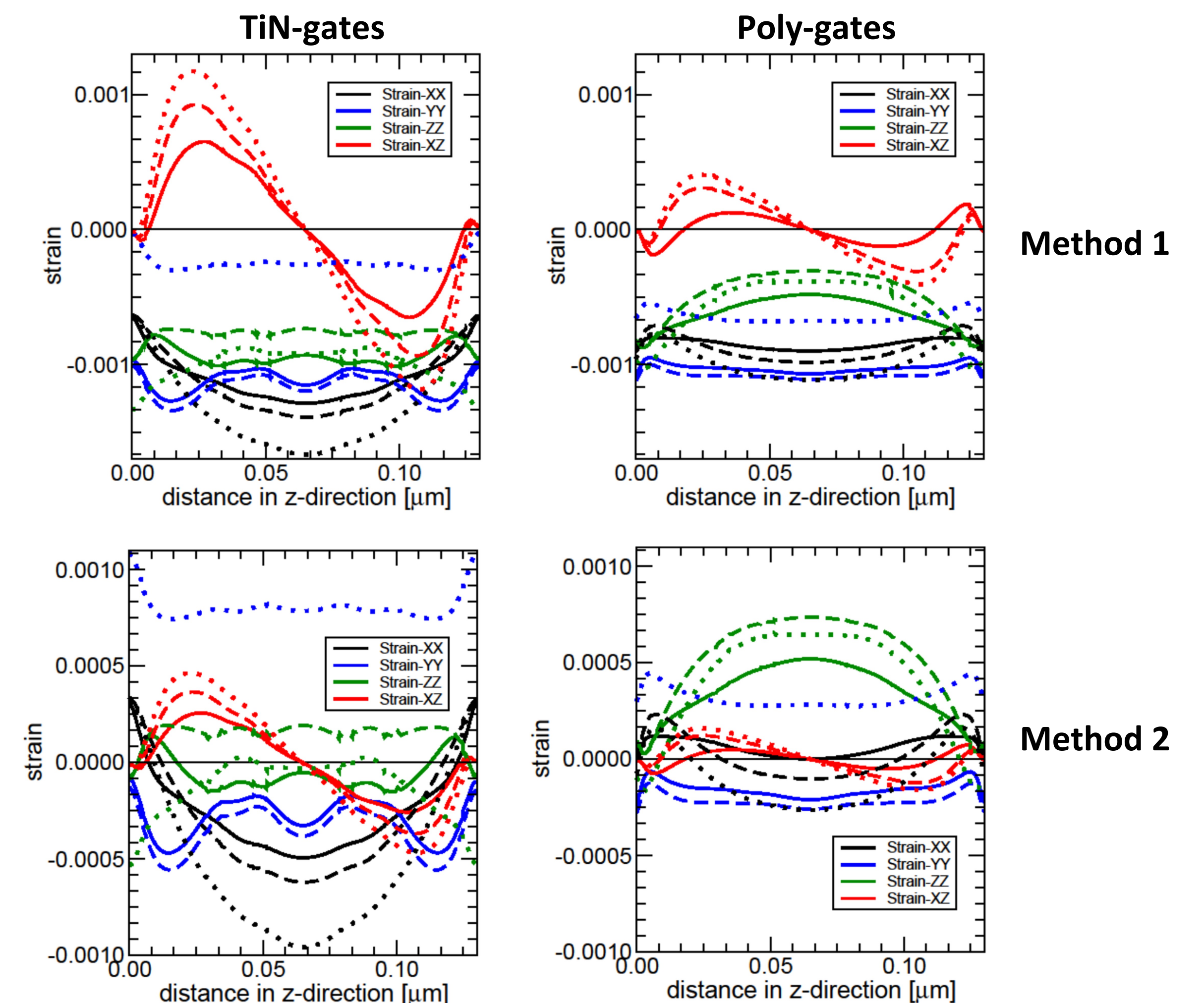## Simulation Results: Strain Profiles along Fin Direction

Figure 4: The four important components of the strain tensor plotted in z-direction through the hole charge centroids at x = 0.036 μm, y = 0. BC Case1 (solid lines), BC Case2 (dashed lines), BC Case3 (dotted lines). Bias configuration adjusted for 1 hole under plunger gate and a "reasonable" z-location: $V_{L1/2}$ = -0.5 V, V_{G1} = -0.675 V, $V_{G2/3}$ = -1.05 V for TiN-gates and $V_{L1/2}$ = +0.3 V, V_{G1} = +0.2 V, $V_{G2/3}$ = -0.25 V for poly-gates p-doped with 5e19 cm^{-3}.

Simulation Results: Impact on Electrostatics

- S-Device is employed to solve for the electrostatics, with the calibrated density gradient model [2] used to capture the quantum confinement effect and with the 6x6 k·p theory (Bir-Pikus model [3]) to compute strain-induced changes of band structure, DOS, and hole charge distribution.
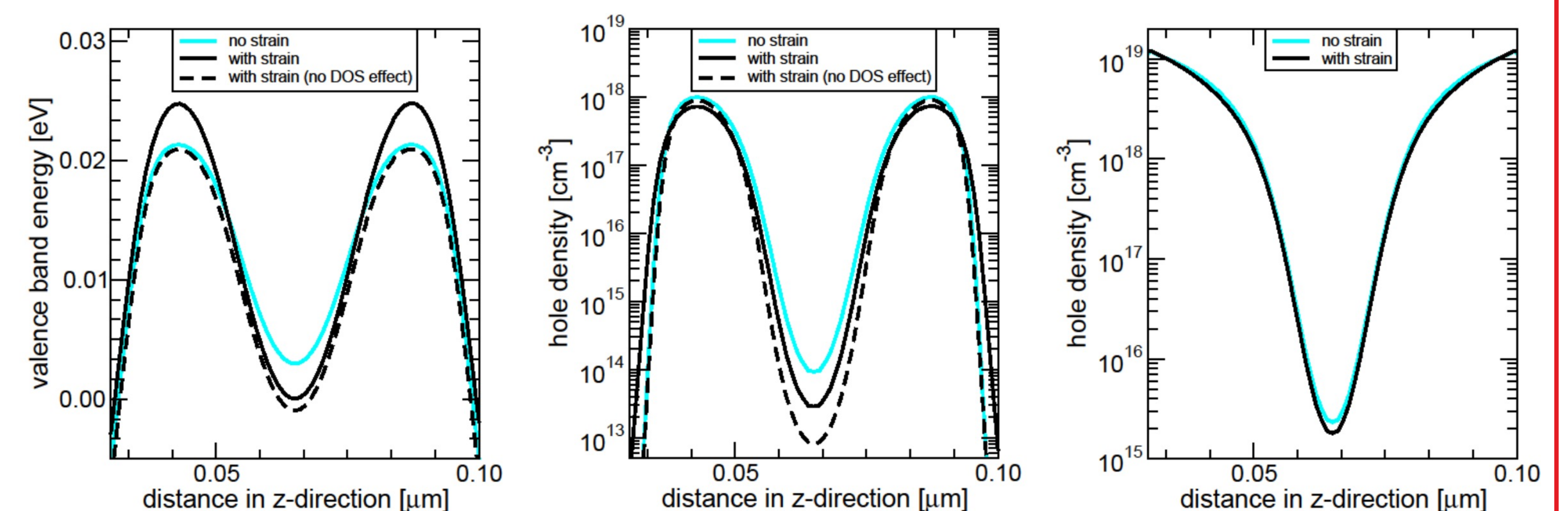

Figure 5: Electrostatics results for TiN-gates, Method1, and BC Case1. (left) Valence band energy at bias configuration as in Fig.4. (middle) Hole density at bias configuration as in Fig.4. (right) Hole density at experimental lead gate voltage $V_{L1/2}$ = -4.5 V. For the dashed curves the strain effect on the DOS was neglected.

Conclusion

- The cooling-induced strain is small compared to strain boosters in CMOS (0.1% *vs* 2%).
- The effect of this strain and its gradients on the total hole charge in the quantum dot is almost negligible, because the hole charge is fixed by the applied bias (neutrality condition in a MOS device).
- The overlap density can change within one order of magnitude, depending on the BCs.
- Poly-gates have a smaller effect than TiN-gates due to their very different expansion coefficients compared to that of SiO$_2$.
- Strain does not help at all to localize a hole under the plunger gates when the applied voltage at the accumulation gates is set as in the experiment (-4.5V).

Acknowledgement

References
1. Camenzind et al., Nature Electronics 5 (2022)
2. Sentaurus-Device Manual, ver. 2023.12
3. G. L. Bir and G. E. Pikus, Symmetry and Strain-Induced Effects in Semicond., Wiley&Sons, 1974