Impact of Floating Body Effect, Back-Gate Traps, and Trap-Assisted Tunneling on Scaled $In_{0.53}Ga_{0.47}As$ Ultrathin-Body MOSFETs and Mitigation Measures

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***Abstract*— Ultrathin-body (UTB) III–V channel MOSFETs are known to suffer from the floating body effect which turns on a parasitic bipolar junction transistor (BJT) and increases the off-state leakage current. This paper presents a TCAD simulation study of UTB $In_{0.53}Ga_{0.47}As$ n-channel MOSFETs with nanowire and planar device geometry, each with different gate lengths (L_G) ranging from 13 to 300 nm. A single set of parameters results in good agreement with measured transfer characteristics of all six different device geometries. The impact of band-to-band tunneling (BTBT), trap-assisted tunneling (TAT), and the electrostatic effect of traps at the buried-Al_2O_3/InGaAs interface has been deconvoluted during the TCAD analysis. It is found that the turn-on of the parasitic BJT is mainly caused by the combined effect of BTBT at the channel–drain junction and TAT at the gate-oxide/drain overlap. Furthermore, it is revealed that traps at the buried-Al_2O_3/InGaAs act as a backgate and degrade the subthreshold swing of the planar MOSFETs. The off-state leakage due to the parasitic BJT could be minimized with the help of an oxide spacer between HfO_2 and InGaAs drain and by introducing a dopant grading at the source–channel and the drain–channel interfaces.**

***Index Terms*— III–V MOSFETs, floating body effect, parasitic bipolar junction transistor (BJT), trap-assisted tunneling (TAT).**

I. Introduction

DUE to superior electron transport properties, InGaAs is gaining more attention as a channel material for future CMOS applications. Increasing the indium content in InGaAs improves the electron mobility but reduces the band gap. The former imparts higher driving capability while the latter is known to increase gate-induced drain leakage due to band-to-band tunneling (BTBT). The intermediate composition $In_{0.53}Ga_{0.47}As$ represents a reasonable compromise. Requirements for high-performance computing call for ultrathin-body (UTB) MOSFETs which offer a small parasitic capacitance. These UTB MOSFETs tend to suffer from the so-called floating body effect [1]–[3] which gives rise to a higher OFF-state leakage current, an abnormal subthreshold swing (SS), current instability in switching operation, etc. In addition, traps at the gate-oxide/InGaAs interface and InGaAs/buried-oxide interface adversely affect the device characteristics.

Yet, the exact mechanisms that deteriorate the MOSFETs device performance have not been analyzed to date. To overcome this gap and hence to be able to help future optimization of such MOSFETs, we present in the following, two sets of $In_{0.53}Ga_{0.47}As$ UTB MOSFETs. These have been analyzed to understand the mechanisms responsible for the OFF-state leakage current and the associated degradation of the SS. The individual physical mechanisms are deconvoluted through simulations to obtain a detailed photograph of how they impact the I–V curves.

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II. Simulation Setup

A. Device Geometry

The two sets of MOSFETs mentioned above were integrated on Si by direct wafer bonding and were fabricated following a CMOS-compatible self-aligned replacement-metal-gate process. Fabrication details are described in [4] and [5]. The UTB MOSFET with a fin width of 17 nm has a nearly circular cross section resulting from the fabrication process [see Fig. 1(d)]. Therefore, it was simulated with the device simulator Sentaurus-Device [6] in 2-D as a nanowire (NW) FET using cylindrical coordinates. As shown in Fig. 1(a), the channel of this NW MOSFET consists of unintentionally n-doped $In_{0.53}Ga_{0.47}As$, whereas the raised source and drain are composed of n-doped $In_{0.53}Ga_{0.47}As$. The device dimensions and the doping profile are marked in Fig. 1(a). The gate

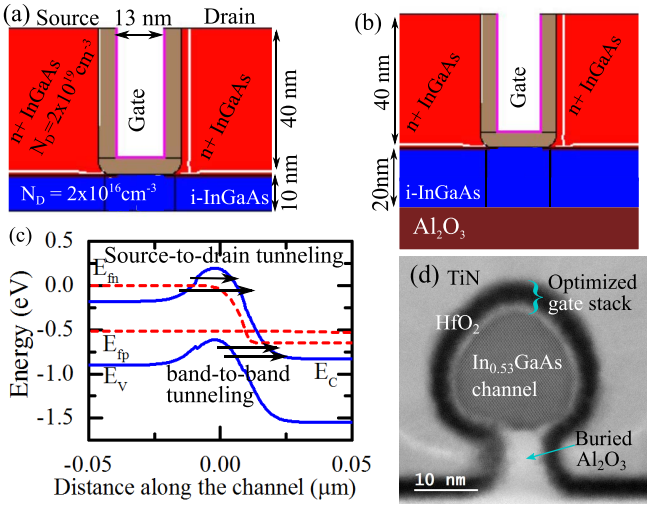

Fig. 1. (a) Axial cross section of the NW MOSFET with $L_G = 13$ nm. (b) Vertical cross section of the planar MOSFET with $W_G = 500$ nm and $L_G = 13$ nm. (c) Band diagram along the axis of the NW MOSFET at $V_{DS} = 650$ mV and $V_{GS} = -250$ mV. Locations of STDT and BTBT are marked. (d) TEM image of the cross section of the NW MOSFET normal to the transport direction.

oxide is an Al_2O_3/HfO_2 bilayer with an equivalent oxide thickness of 8.5 Å extracted from *CV* measurements. Similarly, the planar MOSFET with a channel width of 500 nm was analyzed by simulating a vertical cross section of the device. Device dimensions and doping profile are shown in Fig. 1(b). The planar MOSFET differs from its NW counterpart by the presence of a buried-Al_2O_3/InGaAs interface.

B. Model Parameters

The aim of the simulations was to understand the origin of the high OFF-current and the large SS. Since both depend only weakly on the carrier mobility, the latter was fixed to a constant value of 300 $cm^2/(V \cdot s)$ in planar devices and 80 $cm^2/(V \cdot s)$ in NW devices. As this approach ignores the mobility degradation at high gate bias, it cannot predict the ON-current accurately. The effect of electron rearrangement due to quantum confinement in the channel was taken into account by using the anisotropic density gradient model [7], [8]. The scaling factor γ [6] was calibrated to the electron density profile obtained from a 1-D Schrödinger–Poisson solver which gave $\gamma = 1.5$. Wave function penetration into the oxide was activated in the model. BTBT at the gate–drain junction was modeled by the dynamic nonlocal path BTBT model [9]. Source-to-drain tunneling (STDT) of electrons was modeled by the Wentzel–Kramer–Brillouin-based nonlocal tunneling model available in Sentaurus-Device following the approach used in [10]. The required electron and hole effective masses were set to $m_e = 0.043\ m_0$ and $m_{1h}^{[001]} = 0.052\ m_0$ [11]. Electron and hole lifetimes which determine the Shockley–Read–Hall (SRH) recombination rate were set to 1 ns. Auger recombination was included with Auger coefficients adopted from the experiments in [15] and [16]. Their values were set to $2.5 \times 10^{-28} cm^6 \cdot eV^{-1}$ for both electrons and holes. The work function (WF) of each device was adjusted to match the experimental data. It ranges from 4.65 to 5 eV.

C. Interface Trap Density and Model Parameters

In a long-channel NW MOSFET at $V_{DS} = 50$ mV, the effect of traps at the HfO_2/InGaAs interface on the device characteristics is merely electrostatic. Therefore, D_{it} at the interface was set to $2 \times 10^{12} cm^{-2} \cdot eV^{-1}$ to obtain a good fit to the subthreshold characteristics of the long-channel NW MOSFETs at $V_{DS} = 50$ mV. Following the experimentally extracted distribution of traps at the InGaAs/Al_2O_3 interface reported in [12], the donor-type D_{it} at the back-side interface in the planar MOSFETs was assumed to be uniform with a value of $1.5 \times 10^{12}\ cm^{-2} \cdot eV^{-1}$ throughout the band gap. This distribution of traps was superimposed with a Gaussian profile energetically located at the valence band (VB) edge of InAs with a peak D_{it} of $3 \times 10^{13}\ cm^{-2} \cdot eV^{-1}$ and a full-width-half-maximum of 480 meV.

Trap-assisted tunneling (TAT) at the HfO_2/InGaAs interface was modeled by a nonlocal model [13] after creating a nonlocal mesh normal to the gate–drain overlap. The parameter trap volume in the TAT model was set to 50 $Å^3$, whereas the capture cross section in the multiphonon excitation model was fixed to 50 $Å^2$. Bulk values of the effective masses m_e and m_{1h} were used for the calculation of the tunnel probability in the TAT model.

III. Simulation Results and Discussion

Fig. 2(a)–(f) presents a comparison of the simulated and the experimental transfer characteristics of the NW and the planar MOSFETs, respectively, with different gate lengths. The good match suggests that the simulation setup can include the effects of all leakage mechanisms and traps.

A. Band-to-Band Tunneling and Floating Body Effect

Fig. 3(b) shows a color-mapped diagram of the BTBT rate in the OFF-state of the NW MOSFET with $L_G = 13$ nm. Holes generated in the channel lower the potential in the channel and enhance the forward-biased p-n junction at the source–channel interface. This turns ON a parasitic bipolar junction transistor (BJT), as shown in Fig. 3(a). The hole current is supplied to the base by BTBT generation as represented by a fictitious current source in Fig. 3(a). A color-mapped diagram of the SRH recombination rate confirms that all the holes indeed recombine at the source–channel junction suggesting that the forward-biased p-n junction is active. This effect is prominent at high V_{DS} and is found to be absent at $V_{DS} = 50$ mV. Since the lifetimes $\tau_{e,h}$ in the UTB InGaAs are not known, they are adjusted to match the leakage current. The OFF-current is dominated by BTBT generation and SRH recombination. Since the parameters of BTBT are taken from experiments, adjusting the lifetimes is a reasonable approach. As shown in Fig. 3(b), the leakage current increases with $\tau_{e,h}$ due to increased gain of the parasitic BJT. The device characteristics are found to be unaffected by Auger recombination.

B. Impact of Source-to-Drain Tunneling

Simulations of the short-channel ($L_G = 13$ nm) NW and planar MOSFETs can match the experimental data without activating traps and TAT models at either of the two

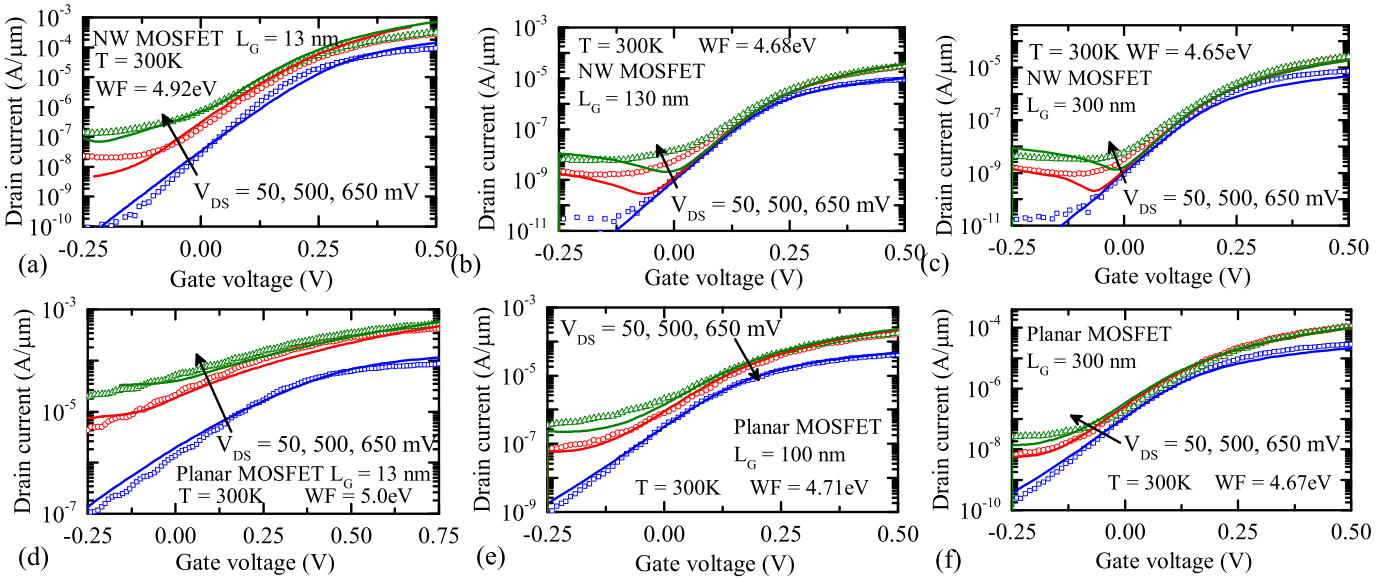

Fig. 2. Comparison of simulated (solid) and experimental (circles) transfer characteristics of (a)–(c) NW MOSFETs and (d)–(f) planar MOSFETs with gate lengths of 13, 100 (planar only), 130 (NW only), and 300 nm.

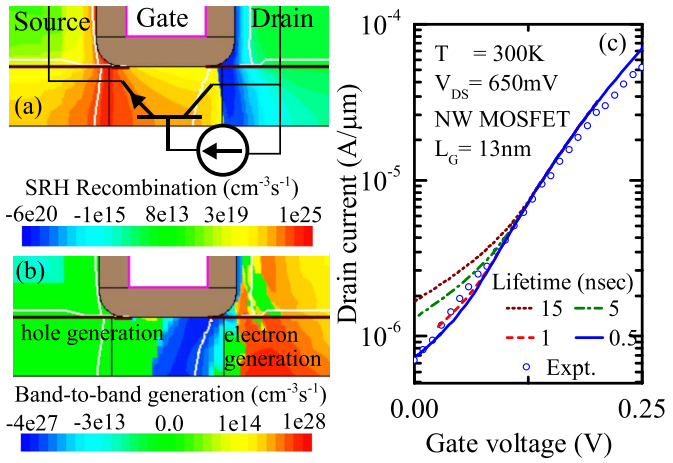

Fig. 3. Contour diagrams of (a) SRH recombination and (b) BTBT generation rates along the axial cross section of the NW MOSFET with L_G = 13 nm. A parasitic BJT is formed as sketched in (a). BTBT in (b) acts as a current source supplying holes to the base of the BJT. (c) Effect of variation of carrier lifetime on the OFF-current.

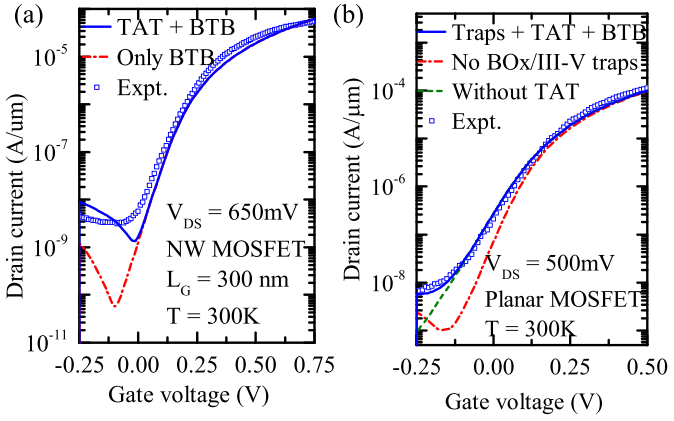

Fig. 4. Transfer characteristics of the long-channel (a) NW MOSFET and (b) planar MOSFET with TAT and without TAT. Transfer characteristics of the planar MOSFET in (b) with and without buried-Al_2O_3/InGaAs traps confirm the degradation of the slope due to back-side traps.

oxide/semiconductor interfaces. Thus, a large parasitic BJT effect in short-channel MOSFETs dominates the leakage current at high V_{DS} [see Fig. 2(a) and (d)]. At V_{DS} = 50 mV, simulations predict a degradation of the SS of the short-channel devices. This could be attributed to STDT, since the traps and the TAT models are not activated in the simulation. As traps are still present in the fabricated devices, this means that the effect of STDT is more dominant than TAT or electrostatic screening of the channel by the HfO_2/InGaAs traps.

A degradation of the SS due to the electrostatic screening of the channel by the traps at HfO_2/InGaAs interface is observed in the long-channel NW MOSFETs in which STDT is absent.

C. Trap-Assisted Tunneling at InGaAs/HfO_2 Interface

The strong negative V_{GD} in the OFF-state of the MOSFETs creates a triangular-like potential well adjacent to the gate–drain overlap region (vertical right-side wall of the gate). As a result, electrons from the VB can undergo multiphonon excitation to the trap levels followed by tunneling into the conduction band [14]. This TAT process causes generation of electron–hole pairs. Electrons flow to the drain adding to the leakage current, while holes drift toward the channel along the interface. In long-channel MOSFETs, this supplies holes to the parasitic BJT. As shown in Fig. 4(a), the OFF-state leakage current in the NW MOSFET with L_G = 300 nm resembles the experimental leakage current as soon as the TAT at the gate–drain overlap region is activated in the simulations. A similar effect is observed for the planar MOSFET with L_G = 300 nm [see blue solid curve versus green dashed curve in Fig. 4(b)].

D. Gain of the Parasitic BJT

The OFF-state leakage may arise from BTBT, TAT, or STDT. In long-channel devices, STDT is negligible due to

the thick tunnel barrier. Therefore, the drain current (I_D) at $V_{GS} = -0.25$ V is the sum of collector current (I_C) and base current (I_B) of the parasitic BJT. Considering this, the gain (β) of the BJT can be calculated as

$$\beta = \frac{I_C}{I_B} = \frac{I_D - I_B}{I_B}. \quad (1)$$

Since BTBT as well as TAT supply holes to the BJT, the base current is the integral of the electron generation rates of BTBT and TAT processes throughout the channel and drain regions of the device

$$I_B = e \int [G_{BTBT}(r) + G_{TAT}(r)] d^2r \quad (2)$$

where e is the elementary charge. For a planar MOSFET with $L_G = 300$ nm, the abovementioned integration yields $I_B = 2.62 \times 10^{-10}$ A/μm. Using I_B and I_D to calculate β, one obtains $\beta \approx 19$ at $V_{GS} = -0.25$ V. Similar calculations result in $\beta \approx 25$ for the planar MOSFET with $L_G = 100$ nm. The gain of the parasitic BJT increases with decreasing channel lengths. This is because the gain of a BJT is inversely proportional to the base width. (The channel acts as the base of a parasitic BJT.) However, the above calculations yield $\beta \approx 10^5$ for the short-channel planar MOSFET with $L_G = 13$ nm. Such an unphysical value of β arises from the violation of the assumption that only the parasitic BJT contributes to the OFF-state leakage current (i.e., $I_D = I_B + I_C$). In the short-channel planar MOSFET, the gate does not control the region at the bottom of the channel. Since the channel region is unintentionally n-doped, current conduction continues near the bottom of the channel at $V_{GS} = -0.25$ V, resulting in a large leakage current. Since this leakage mechanism is not taken into account in the abovementioned calculation, it yields an unphysically high β.

E. Effect of Back-Gate Traps at Al_2O_3/InGaAs Interface

Planar MOSFETs have a buried-Al_2O_3/InGaAs interface with a large donor D_{it}. Due to the absence of a triangular-like potential well at this interface, no TAT takes place. However, the traps are occupied/emptied by a multiphonon excitation process when the Fermi level in the channel is changed by the gate bias. Because of the large D_{it} [12], this interface carries a high sheet charge and acts as a weakly controlled backgate. Electrons are attracted to the positively charged traps and accumulate in the channel. As a result, the channel remains conductive even at low gate bias. In this way, back-gate traps reduce the gate control of the channel and degrade the SS. Transfer characteristics of the planar MOSFET with $L_G = 300$ nm show a degradation of the SS as soon as the Al_2O_3/InGaAs traps are activated in the simulations. This effect is also present in the NW MOSFETs, but to lesser extent due to the narrow Al_2O_3/InGaAs interface at the bottom of the NW noticeable in the TEM image [see Fig. 1(d)]. Our simplified 2-D simulations with cylindrical coordinates cannot capture this effect. Therefore, a slight disagreement between simulated and experimental data of the long-channel InGaAs NW MOSFETs is observed around $V_{GS} = 0$ V in Fig. 2(b) and (c). A 3-D simulation of the actual geometry could reproduce this effect.

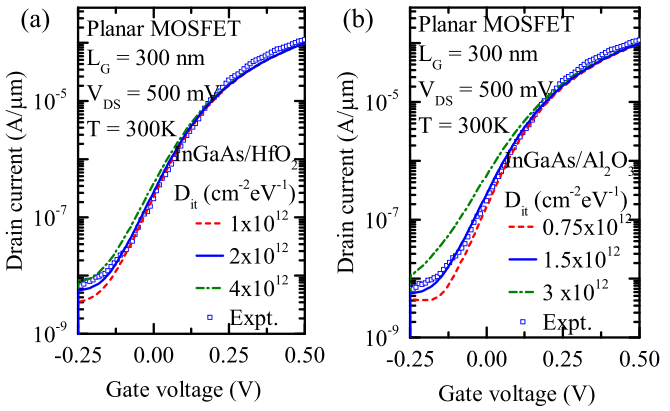

Fig. 5. Transfer characteristics of the planar MOSFET obtained by changing D_{it} at (a) InGaAs/HfO_2 and (b) InGaAs/Al_2O_3 interface by factors of 0.5 and 2, respectively. Variation of D_{it} at the InGaAs/HfO_2 interface has a rather small effect on the *I–V* plots.

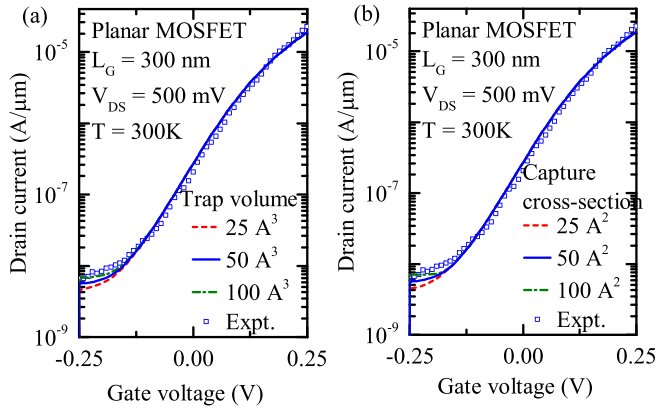

Fig. 6. Transfer characteristics simulated by varying (a) trap volume (needed in the TAT model) and (b) capture cross section (needed in the multiphonon excitation model) by factors of 0.5 and 2, respectively.

F. Sensitivity Analysis of Trap Parameters

In the abovementioned analysis, D_{it}, trap volume, and capture cross section at the InGaAs/HfO_2 interface have been adjusted for a good match with the experimental transfer characteristics. In the long-channel NW MOSFETs, only D_{it} affects the electrostatics, which in turn increases the SS. Using this property, D_{it} was extracted to match the swing in the subthreshold region. The remaining parameters were taken from [14]. Simulations were carried out to assess which impact a variation of each parameter in the conclusions of this work. The transfer characteristics of a planar MOSFET with $L_G = 300$ nm obtained by doubling and halving D_{it}, active trap volume, and capture cross section are presented in Figs. 5(a) and 6(a) and (b), respectively. The results suggest that an error in the determination of D_{it} would introduce a small uncertainty in the subthreshold region, whereas the variations of active trap volume and capture cross section have almost negligible effect on the OFF-current at $V_{GS} = -0.25$ V.

D_{it} at the InGaAs/Al_2O_3 interface has been modeled based on a measured distribution [12]. However, it might be different in the devices studied here due to a different process flow. The transfer characteristics obtained by doubling and halving the uniform D_{it} at the InGaAs/Al_2O_3 are shown in Fig. 5(b). The current is sensitive to an increase of D_{it}, but does not alter significantly when D_{it} is lowered.

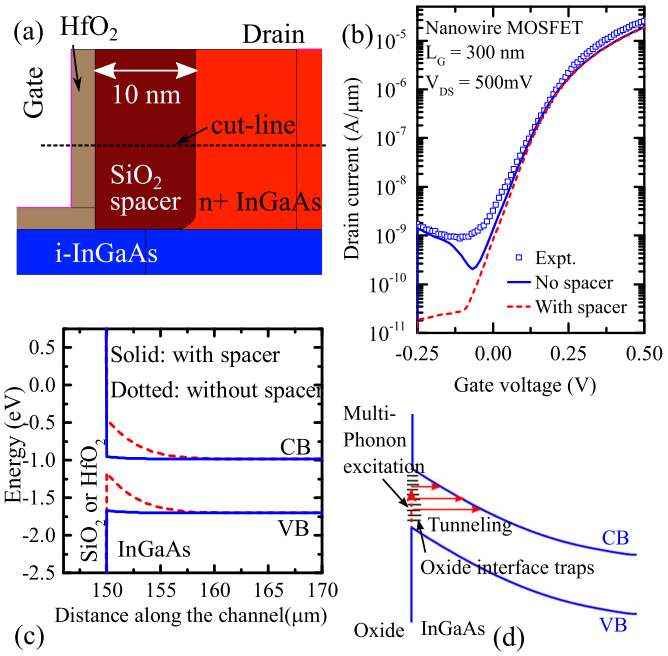

Fig. 7. (a) Part of the device including a spacer on the drain side. (b) Comparison of the transfer characteristics of the NW MOSFET with and without spacers. (c) Band-edge diagrams along the cutline shown in (a) with and without spacers. The semiconductor/oxide interfaces were aligned. (d) Schematic showing that TAT can occur only when a triangular potential well is present at the oxide/InGaAs interface.

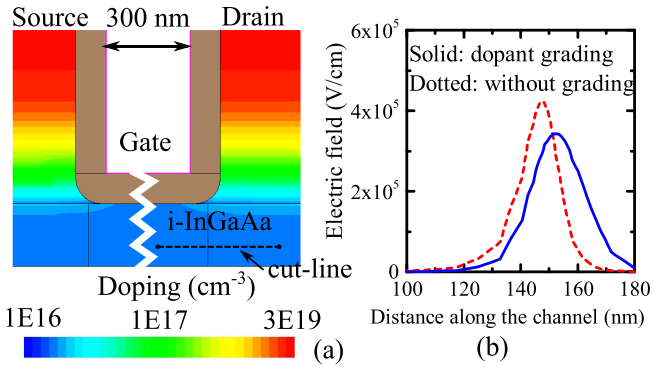

Fig. 8. (a) Dopant grading introduced at the source and the drain. (b) Electric field along the cutline shown in (a).

As observed in Figs. 5 and 6, uncertainties in trap concentration, trap volume, and capture cross section do not change the transfer characteristics to an extent that would foil the conclusions of this work.

IV. Mitigation of Floating Body Effect

A. Suppression of TAT at InGaAs/HfO$_2$ Interface

In an NW MOSFET under low gate bias ($V_{GS} < 0$ V), TAT at the InGaAs/HfO$_2$ interface results in hole generation at the HfO$_2$/InGaAs-drain interface. These holes drift to the channel and enhance the leakage due to the floating body effect. A thick-SiO$_2$ spacer between HfO$_2$ and n+ InGaAs in the drain [as shown in Fig. 7(a)] can reduce the leakage current by 2 orders of magnitude as shown by the transfer characteristics of the long-channel ($L_G = 300$ nm) NW MOSFET with and without spacers [see Fig. 7(b)]. This is achieved by suppression of TAT at the InGaAs-drain/HfO$_2$ interface. In the OFF-state, a large $V_{GD} = -0.9$ V gives rise to a hole inversion layer at the interface. A SiO$_2$ spacer causes a gradual drop of the potential across the low-k spacer. This prevents the formation of a triangular well and a hole inversion layer at the interface. The band diagram along a cutline [dotted line in Fig. 7(a)] normal to the drain/oxide interface was extracted and plotted in Fig. 7(c). It confirms that the triangular well vanishes as soon as an oxide spacer is introduced. Consequently, the tunneling step of the TAT process [Fig. 7(d)], which requires a triangular potential well at the interface, becomes infeasible. This inhibits TAT at the InGaAs/HfO$_2$ interface and, in turn, reduces the OFF-state leakage. Note that the same trap distribution was used at the oxide/semiconductor interface with and without the spacer, respectively. Simulations suggest that the spacer thickness of 10 nm is sufficient to minimize TAT at oxide/InGaAs interface. Leakage does not reduce further if a thicker spacer is used. Also, the spacer creates an additional series resistance which could reduce the ON-current. This effect is minimal in a long-channel MOSFET with $L_G = 300$ nm due to the high channel resistance.

B. Dopant Grading in Source and Drain

In the original devices, the doping changes nearly abruptly between channel and source/drain. If dopant atoms were introduced gradually during the growth of InGaAs, a gradual i-n+ junction would form. In the simulations, a dopant grading of Gaussian shape was used over a distance of 20 nm above the channel, as shown in Fig. 8(a). The gradual doping alters the electrostatics of the device. The peak of the electric field along the channel/drain interface is lowered, and the field spreads over larger distance [see Fig. 8(b)]. As a result, BTBT between channel and drain becomes weaker. Also, due to the reduced n-type doping adjacent to the vertical HfO$_2$/InGaAs interface, the triangular well does not form or it is shallower compared to the original devices with high doping. As a result, the tunneling barrier widens which reduces TAT at the HfO$_2$/InGaAs interface. Both the abovementioned effects reduce the supply of holes to parasitic BJT, and the OFF-state leakage is reduced. Transfer characteristics obtained by changing thickness of the grading region are compared in Fig. 9. The simulations show that increasing thickness of the grading region which is same as reducing steepness of Gaussian profile decreases the OFF-state leakage current.

The abovementioned techniques indeed reduce the OFF-state leakage of a long-channel MOSFET. The same modifications were employed in the simulated short-channel ($L_G = 13$ nm) NW MOSFET. Its transfer characteristics are compared with those of the original device in Fig. 10. Although the proposed mitigations reduce the OFF-state leakage, they also result in a severe reduction of the ON-current due to the additional parasitic resistances. Besides, V_T-shift is observed in the short-channel MOSFETs, after introducing dopant grading in the source and the drain. It is due to change in the electrostatics and the capacitances. Such a V_T-shift is not observed in the long-channel MOSFETs. Due to the long channel, the relative

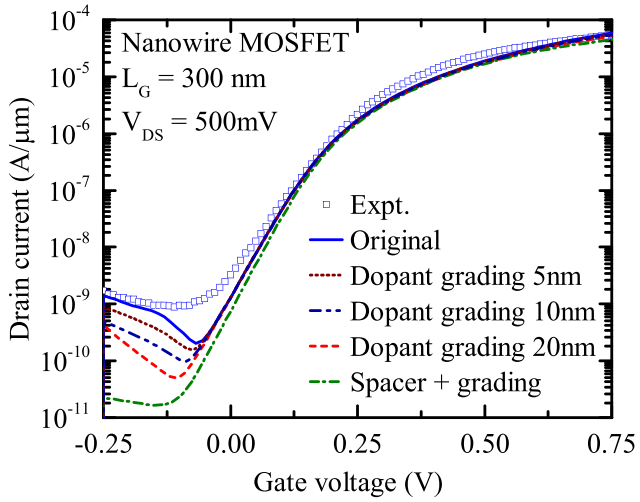

Fig. 9. Comparison between the transfer characteristics of original long-channel NW MOSFETs of $L_G = 300$ nm with the modified devices obtained by introducing dopant grading as well as spacer in the original devices.

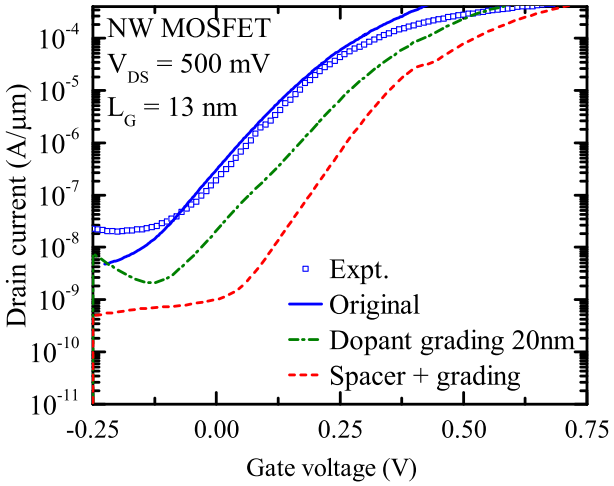

Fig. 10. Comparison between the transfer characteristics of original short-channel NW MOSFETs of $L_G = 13$ nm with the modified devices obtained by introducing dopant grading as well as spacer in the original devices.

change in the capacitance after employing the dopant grading is small in the long-channel MOSFETs, and hence, V_T-shift is negligible. V_T-shift in the short-channel MOSFETs may be compensated by intentionally doping the channel or by gate-WF engineering.

V. Conclusion

A detailed analysis of the InGaAs UTB MOSFETs reveals that channel–drain BTBT as well as TAT at the HfO_2/InGaAs interface at the gate–drain overlap region are responsible for the activation of the parasitic BJT resulting in a large OFF-state leakage current at high V_{DS}. STDT is shown to be responsible for the degradation of the SS in short-channel devices at $V_{DS} = 50$ mV. D_{it} at the buried-Al_2O_3/InGaAs interface deteriorates the SS in planar MOSFETs.

The floating body effect can be mitigated by introducing a SiO_2 spacer between HfO_2 and InGaAs drain and by a dopant grading. Both techniques together reduce the OFF-state leakage of a long-channel NW MOSFET by 2 orders of magnitude. However, they also degrade the ON-current in a short-channel MOSFET.

References

[1] M. Yoshimi *et al.*, "Suppression of the floating-body effect in SOI MOSFET's by the bandgap engineering method using a $Si_{1-x}Ge_x$ source structure," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 423–430, Mar. 1997.

[2] J. G. Fossum, R. Sundaresan, and M. Matloubian, "Anomalous sub-threshold current-voltage characteristics of n-channel SOI MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-8, no. 11, pp. 544–546, Nov. 1987.

[3] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Off-state leakage induced by band-to-band tunneling and floating-body bipolar effect in InGaAs quantum-well MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1203–1205, Dec. 2014

[4] H. Hahn *et al.*, "A scaled replacement metal gate InGaAs-on-Insulator n-FinFET on Si with record performance," in *Proc. IEEE IEDM*, Dec. 2017, pp. 17.5.1–17.5.4.

[5] V. Deshpande *et al.*, "First demonstration of 3D SRAM through 3D monolithic integration of InGaAs n-FinFETs on FDSOI Si CMOS with inter-layer contacts," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2017, pp. T74–T75, doi: 10.23919/VLSIT.2017.7998205.

[6] *Sentaurus Device User Guide, Version 2016.03*, Synopsys Inc, Mountain View, CA, USA, 2016.

[7] M. G. Ancona and H. F. Tiersten, "Macroscopic physics of the silicon inversion layer," *Phys. Rev. B, Condens. Matter*, vol. 35, no. 15, pp. 7959–7965, 1987, doi: 10.1103/PhysRevB.35.7959.

[8] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B, Condens. Matter*, vol. 39, no. 13, pp. 9536–9540, 1989, doi: 10.1103/PhysRevB.39.9536.

[9] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, no. 1, pp. 83–91, 1961.

[10] A. Szabó and M. Luisier, "Under-the-barrier model: An extension of the top-of-the-barrier model to efficiently and accurately simulate ultrascaled nanowire transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2353–2360, Jul. 2013, doi: 10.1109/TED.2013.2263386.

[11] I. R. Vurgaftman, R. J. Meyer, and L. R. Ram-Mohan, "Band parameters for III-V compound semiconductors and their alloys," *J. Appl. Phys.*, vol. 89, no. 11, pp. 5815–5875, 2001, doi: 10.1063/1.1368156.

[12] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces," *Appl. Phys. Lett.*, vol. 95, no. 20, p. 202109, 2009, doi: 10.1063/1.3267104.

[13] A. Palma, A. Godoy, J. A. Jiménez-Tejada, J. E. Carceller, and J. A. López-Villanueva, "Quantum two-dimensional calculation of time constants of random telegraph signals in metal-oxide–semiconductor structures," *Phys. Rev. B, Condens. Matter*, vol. 56, no. 15, pp. 9565–9574, 1997, doi: 10.1103/PhysRevB.56.9565.

[14] S. Sant *et al.*, "Lateral InAs/Si p-Type tunnel FETs integrated on Si—Part 2: Simulation study of the impact of interface traps," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4240–4247, Nov. 2016, doi: 10.1109/TED.2016.2612484.

[15] S. Hausser, G. Fuchs, A. Hangleiter, and K. Streubel, "Auger recombination in bulk and quantum well InGaAs," *Appl. Phys. Lett.*, vol. 56, no. 10, p. 913, 1990, doi: 10.1063/1.103175.

[16] M. E. Prise, M. R. Taghizadeh, S. D. Smith, and B. S. Wherrett, "Picosecond measurement of Auger recombination rates in InGaAs," *Appl. Phys. Lett.*, vol. 45, no. 6, p. 652, 1984, doi: 10.1063/1.95344.

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