Simulation Study of Nanowire Tunnel FETs

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Tunnel FETs (TFETs) are candidates for low-power logic switches with sub-thermal slope which could enable a strongly reduced supply voltage. To improve the ON-current compared to Si TFETs, III-V/Si hetero junctions have been proposed [1]. Using nanowires has additional advantages: (i) the possibility of many different material combinations [2], (ii) efficient strain relaxation in the case of small diameters [2], (iii) a good electrostatic control due to the surrounding gate. Tomioka et al. [3,4,5] and Björk et al. [6] have advanced the integration of InAs nanowires on Si with nanometer-scale hetero epitaxy. The present simulation study refers to their experimental data.

The combined application of a quantum transport solver and a TCAD tool can help to understand the behavior of InAs/Si hetero nanowire Esaki diodes and TFETs and can give guidelines to improve their performance by optimization of geometry, doping, gating, and biasing. We used the quantum transport simulator OMEN [7] which is massively parallel, multi-dimensional, atomistic, and based on a $sp^3d^5s^*$ tight-binding representation of the band structure. Quantum transport simulation can be done either in the Non-equilibrium Greens Function (NEGF) formalism (scattering) or in the Wave Function formalism (ballistic). OMEN has been applied to direct and phonon-assisted band-to-band tunneling (BTBT) in InAs, Si, and Ge nanowire homo TFETs [8]. The commercial device simulator Sentaurus-Device [9] is equipped with various local and non-local BTBT models. Neither a theory nor an analytical model for BTBT in a hetero junction between a direct and an indirect semiconductor exists. A practical workaround has to be used with S-Device, since a tunnel path across the hetero interface must either belong to a direct (zero-phonon) or to a phonon-assisted tunnel process. Therefore, (i) the "*dynamic nonlocal path BTBT model*" (short cut: "*Kane model*" [10]), calibrated for InAs, is also used on the silicon side, fitted to experimental data of [11], and (ii) the calibrated model for Si [12] (short cut "*Schenk model*") is also used on the InAs side after proper modifications [13].

The BTBT current of short, unconfined Esaki homo diodes ($\langle 111\rangle$, 20 nm length, abrupt doping) was simulated with OMEN for different materials and doping levels. For the direct materials (InAs, GaSb) and for Ge, where coherent BTBT is dominant [8], the simulation of bulk diodes is straightforward. Bulk simulations are needed because there is also no geometrical confinement in the fabricated nanowire TFETs (diameters in the range 25 nm – 100 nm). Fig. 1 shows that InAs has the highest BTBT current density, followed by GaSb and Ge. The upper limit for InAs is $\sim 5\times 10^4$ kA/cm^2. In the case of Si, due to the demanding electron-phonon coupling, at least one-dimensional confinement is necessary (the direction of confinement is $\langle \bar{1}10\rangle$, periodic continuation was applied in $\langle 11\bar{2}\rangle$ direction). The bulk limit of Si remains below 100 kA/cm^2, a factor 500 smaller than that of InAs. Fig. 2 presents the comparison between OMEN and S-Device simulations of InAs Esaki diodes using the calibrated TCAD models. Based on the good agreement, the doping levels at the InAs side of InAs/Si nanowire hetero Esaki diodes produced at IBM Research-Zurich [13,14] were determined by reverse modeling (Fig. 3). Measured [5] and simulated InAs/Si nanowire TFET I_DV_{GS} characteristics are compared in Fig. 5. The striking features of the measured IV curves are: an almost constant slope over 2-3 orders of magnitude, very weak ambipolarity, and a strong saturation of the ON-current for each source-drain voltage. In contrast, simulation yields much higher ON-currents, a strong ambipolarity, curved slopes typical for BTBT, a minimum point slope of 45 mV/dec, and no ON-current saturation. The most likely explanation of the measured currents is that they are dominated by defect-assisted tunneling (DAT), either during interface or bulk SRH generation (Fig. 7). Although multi-phonon coupling parameters of the involved defects in InAs are not known, the shape of the I_DV_{GS} curves can be qualitatively reproduced with a physics-based DAT model [15] in S-Device (Fig. 8). We attribute the absence of BTBT in the measurement to compressive biaxial strain in the highly lattice mismatched system (Fig. 9).

References [1] A. S. Verhulst et al., IEEE Electron Device Lett. 29, 1398 (2008). [2] M. T. Björk et al., Appl. Phys. Lett. 80, 1058 (2002). [3] K. Tomioka et al., Nano Lett. 8, 3475 (2008). [4] K. Tomioka et al., Nanotechnology 20, 145302 (2000). [5] K. Tomioka et al., Appl. Phys. Lett. 98, 083114 (2011). [6] M. T. Björk et al., Appl. Phys. Lett. 97, 163501 (2010). [7] M. Luisier et al., Phys. Rev. B 74, 205323 (2006). [8] M. Luisier et al., J. Appl. Phys. **107**, 084507 (2010). [9] Synopsys Inc., Sentaurus-Device User Guide, Version 2011.09, Mountain View, California, (2011). [10] E. O. Kane, J. Phys. Chem. Solids **12**, 181 (1959). [11] P. M. Solomon et al., J. Appl. Phys. **95** (10), 5800 (2004). [12] A. Schenk, Solid-State Electronics **36** (1), 19 (1993). [13] A. Schenk et al., Proc. SISPAD, 263 (2011). [14] C. D. Bessire et al., Nano Lett. 11 (10), 4195 (2011). [15] A. Schenk, Solid-State Electronics **35** (11), 1585 (1992). [16] C. G. Van de Walle, Phys. Rev. B **39** (3), 1871 (1989).

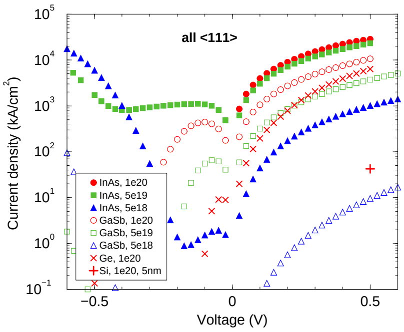

Fig. 1: Short Esaki (bulk) diodes with symmetrical doping simulated with OMEN. The single data point for Si was obtained for a 5 nm slab and took 5 h on Jaguar Cray XK6 using ∼ 20'000 CPUs.

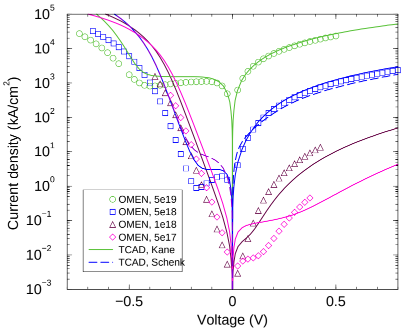

Fig. 2: Comparison between OMEN and S-Device simulations of short InAs Esaki (bulk) diodes with symmetrical doping as indicated. Good agreement is found in the high-doping (high-field) range.

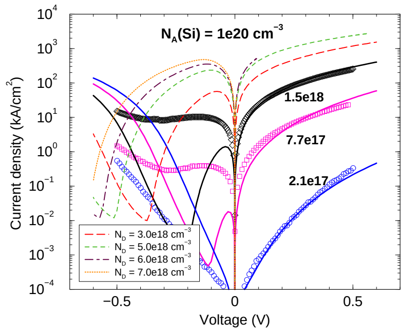

Fig. 3: Comparison between measured and TCAD-simulated InAs/Si nanowire hetero Esaki diodes. The ON-current is limited to $\sim 1 \times 10^4$ kA/cm^2, in good agreement with the homo diodes of Fig. 1.

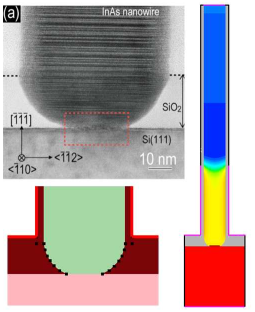

Fig. 4: TEM image of the InAs/Si nanowire TFET from Tomioka et al. [5] (upper left), simulation close-up (lower left), entire simulation domain with carrier concentrations (right).

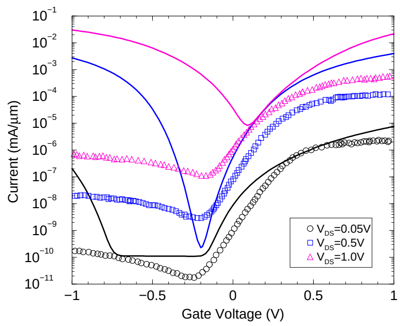

Fig. 5: Measured [5] and simulated InAs/Si nanowire TFET $I_D V_{GS}$ characteristics. Doping according to [5]. Work function = 4.65 eV, EOT = 4.5 nm.

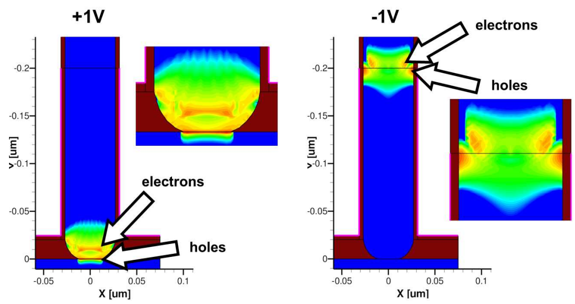

Fig. 6: BTBT rate distribution at V_{GS} =1 V (left) and V_{GS} =-1 V (right). The strong ambipolar current is caused by off-junction tunneling under the gate edge which is aligned with the high-low doping transition. It can be suppressed by a corresponding gate "underlap". The simulated ON-current at V_{GS} =1 V originates from in-junction BTBT with delta-like hole generation at the interface.

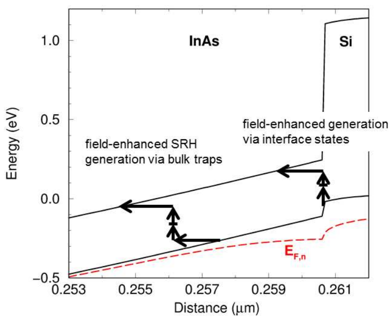

Fig. 7: Band edge profile (solid) and electron quasi Fermi level (dashed) in the vicinity of the hetero junction. Schematic of defect-assisted tunneling during SRH generation.

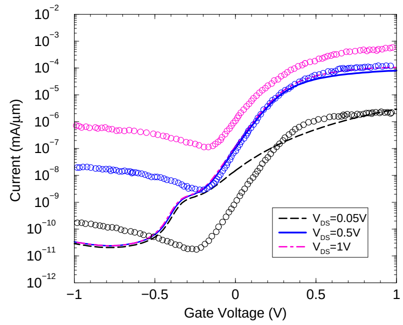

Fig. 8: Simulation with bulk DAT in restricted region (BTBT turned off). DAT parameters: zero-field lifetimes $\tau_n = \tau_p = 3 \times 10^{-8}$ s, lattice relaxation energy $S\hbar\omega_0 = 10.5$ meV, tunnel masses $m_n = 0.023\, m_0$, $m_h = 0.2\, m_0$.

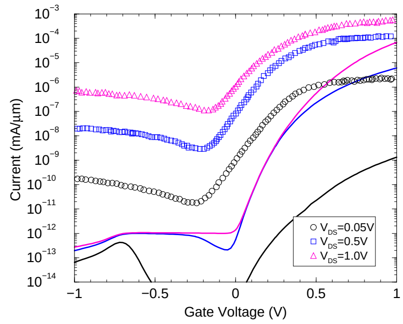

Fig. 9: Measured $I_D V_{GS}$ characteristics [5] and simulated BTBT current assuming homogeneous 8% compressive in-plane strain. Gap extracted from Van de Walle model [16], effective masses from OMEN [7].