Scalability of FinFETs and Unstrained–Si/Strained–Si FDSOI–MOSFETs

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Abstract

Full–band Monte Carlo simulations are performed for n–type FinFETs as well as for unstrained–Si and strained–Si fully–depleted (FD) SOI–MOSFETs. Gate lengths of 50 nm down to 10 nm are considered, and a fixed off–current of 100 nA/μm is in each case ensured by adjusting the silicon film thickness. The FinFET shows the best scaling trend, but the strained–Si FDSOI–MOSFET always involves the largest absolute value for the on–current. However, the on–current decreases upon scaling to 10 nm which might stem from a larger influence of surface roughness scattering in thin Si films affecting most strongly quasi–ballistic transport in strained Si. The feature of a decreasing current is found to be absent in drift–diffusion simulation because this approach does not include quasi–ballistic transport.

1 Introduction

Scaling of bulk MOSFETs into the nanometer regime involves a strong increase of the off–current I_{off} and it is questionable whether further enhancements of the on–current I_{on} can be achieved with an acceptable leakage current level. Alternatives with experimentally confirmed promising scaling properties are strained–Si bulk MOSFETs [1, 2] with enhanced performance and double–gate FinFETs [3, 4] or fully–depleted silicon–on–insulator (FDSOI) MOSFETs [5] with suppressed short–channel effect. Recently, also the fabrication of strained–Si directly on insulator (SSDOI) MOSFETs with eliminated SiGe buffer was reported [6, 7]. However, it is not yet clear which device type will offer the best performance for a fixed, sufficiently low I_{off} when scaled down to 10 nm. Simulation is best suited to address this issue because it is possible to ensure exact comparability, but systematic Monte Carlo (MC) scaling studies have so far been restricted to bulk MOSFETs and gate lengths above about 50 nm [8, 9, 10]. It is therefore the aim of this paper to compare the scalability of FinFETs, unstrained–Si and strained–Si FDSOI–MOSFETs by full–band MC simulation. Results of drift–diffusion (DD) simulations are also shown, because this is still the approach mostly used in industry [11].

2 Scaling Methodology

Figures 1 and 2 show the top view of the FinFET with its angled extension regions [3, 4] and the cross–section of the FDSOI–MOSFET, respectively. In the case of the strained–Si FDSOI–MOSFET it is assumed that the strain–defining relaxed $Si_{0.8}Ge_{0.2}$ buffer can be removed with the technique applied in [6, 7]. Upon scaling the gate length

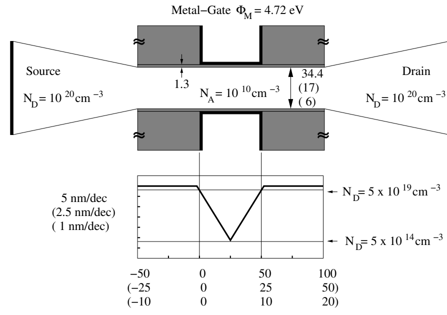

Fig. 1: Top view and doping profile of the FinFET. The gate length L_G is scaled from 50 to 10 nm, the silicon film thickness t_{Si} is from 34.4 to 6.0 nm and the doping steepness from 5 to 1 nm/dec. The spacer length and the source/drain region length are reduced proportional to L_G. The channel direction is in the standard $\langle 110 \rangle$ direction.

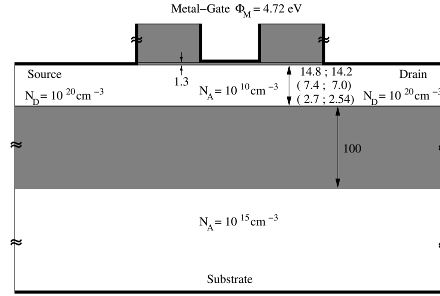

Fig. 2: Cross–section of the FDSOI–MOSFETs. Doping profiles and length scaling are the same as for the FinFET in Fig. 1 except for the silicon film thickness t_{Si} which is scaled from 14.8 (14.2) to 2.7 (2.54) nm for an unstrained (strained) Si channel.

L_G is decreased from 50 to 10 nm. The source/drain region and spacer lengths as well as the steepness, with which the doping falls off into the undoped channel, are reduced correspondingly. For each device configuration, the silicon film thickness t_{Si} is chosen such that I_{off} = 100 nA/μm at a drain voltage of V_{DS}=0.9 V, which is appropriate for high–performance applications [11]. This involves a thinner silicon film in the strained–Si FDSOI–MOSFET in order to compensate for an increased I_{off} under strain which is especially due to the smaller band gap. I_{off} is computed by a DD simulator with a modified work function to account for the quantum mechanical threshold shift as obtained by coupled 1D–Schrödinger–DD simulations. The investigation of the on–state is performed by the full–band MC simulator SPARTA [9]. Note that we have neglected effects such as source–to–drain and band–to–band tunneling which are expected to influence especially the off–state of the shortest device; hence, our results will become quantitatively inaccurate in the most extreme device configurations. However, quasi–ballistic transport is one major aspect of nanoscale device operation in the on–state, so that it is important to explore its scaling behavior also in the limiting case.

3 Simulation Results

In Fig. 3, I_{on} is displayed as a function of L_G for the three device types. The drain current of the double–gate FinFET is divided by two, thus accounting for the double device width and hence double gate capacitance, in order to enable a comparison with the single–gate FDSOI–MOSFETs. The DD models for the bulk mobility in unstrained and strained Si are obtained from corresponding MC bulk simulations and the surface mobility is always adjusted to yield the same drain current as the MC simulation at a drain voltage of V_{DS}=0.05 V. The MC simulations exhibit different scaling behaviors of the device types investigated. While the enhancement of I_{on} continues for the FinFET upon scaling, it becomes weaker for the FDSOI–MOSFET and is even reduced for the

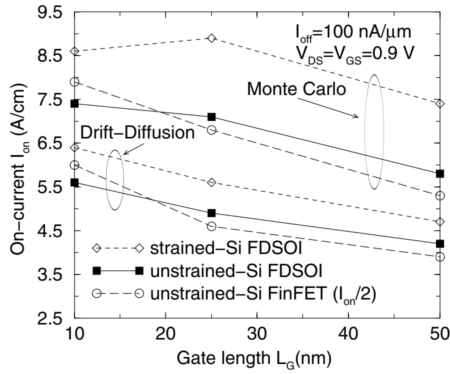

Fig. 3: Gate length dependence of the on–current I_{on} of the FinFET as well as the unstrained–Si and strained-Si FDSOI-MOSEFTs according to Monte Carlo and drift–diffusion simulations. The off–current I_{off} is kept constant at 100 nA/μm.

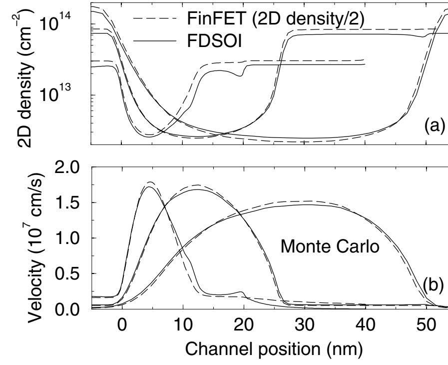

Fig. 4: Profiles along the channel of (a) the electron sheet density obtained by integration of the density perpendicular to the Si/SiO_2 interface and (b) the averaged electron velocity in the FinFET and the unstrained–Si FDSOI-MOSEFT according to Monte Carlo simulation.

strained device featuring, however, still the highest absolute I_{on} at L_G=10 nm. DD not only underestimates I_{on} in the order of 50 %, but also fails to capture the qualitative feature of a decreasing I_{on} in the strained–Si FDSOI–MOSFET upon scaling to 10 nm. These results can be explained by the profiles of electron sheet density and drift velocity along the channel. In Fig. 4, the corresponding MC profiles in the FinFET and the FDSOI–MOSFET are compared for all three gate lengths. The velocities in the source–side of the channel are always almost the same, whereas the source–side sheet density of the FDSOI–MOSFET becomes smaller upon scaling and explains the smaller I_{on} at L_G=10 nm. The opposite situation is present in Fig. 5, where the MC results for unstrained–Si and strained–Si FDSOI–MOSFETs are compared. The strain–enhanced I_{on}'s are due to higher source–side velocities with the source–side sheet densities being similar. However, the velocity improvement for strained–Si upon scaling to L_G=10 nm is no longer strong enough to compensate the reduced sheet density so that I_{on} becomes smaller. This may stem in part from an increasing influence of surface roughness scattering on a largely ballistically determined velocity at very small t_{Si}. Finally, DD and MC results are shown in Fig. 6 for the strained–Si FDSOI–MOSFET. We ascribe the increase of the DD–I_{on} and the decrease of the MC–I_{on} to two points. On the one hand, the absence of quasi–ballistic transport in DD prevents the detrimental impact of surface roughness scattering to become effective. On the other hand, the MC velocity overshoot peak is shifted from the drain– to the source–side for smaller L_G which involves also a decrease of the source–side sheet density (In the short device the electrons are very hot at the drain-side; hence scattering there is strong reducing the drain–side velocity. The importance of scattering in the drain–side for short devices has also recently been stressed in [12]).
In conclusion, the double–gate FinFET has been found to be the device with the best scaling behavior, while the strained–Si FDSOI–MOSFET has been confirmed to yield

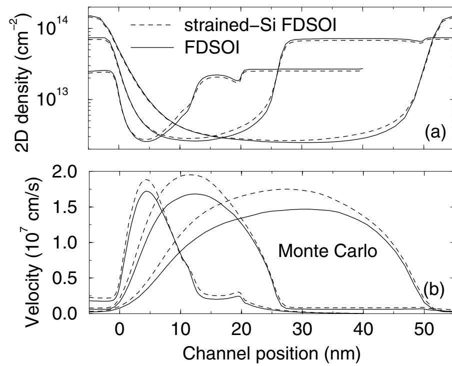

Fig. 5: Profiles along the channel of (a) the sheet density and (b) the averaged velocity in the unstrained–Si and the strained–Si FDSOI-MOSEFT according to Monte Carlo simulation.

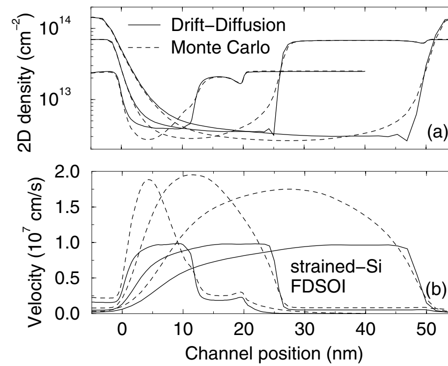

Fig. 6: Profiles along the channel of (a) the sheet density and (b) the averaged velocity in the strained–Si FDSOI-MOSEFT according to Monte Carlo and drift–diffusion simulations.

the highest absolute current levels. This suggests that some kind of strained–Si double–gate MOSFET should theoretically lead to a maximum performance. From a technological viewpoint the FinFET seems an unlikely candidate and it remains to see whether such a device type can be more easily fabricated in some other structure.

Acknowledgments

We would like to thank M. Städele for useful discussions. Financial support by Fujitsu Laboratories Ltd. (Akiruno, Japan) is gratefully acknowledged.

References

[1] J.-S. Goo *et al.*, IEEE Electron Device Lett. **24**, 351 (2003).

[2] T. Sanuki *et al.*, *IEDM Tech. Dig.*, 65 (2003).

[3] B. Yu *et al.*, *IEDM Tech. Dig.*, 251 (2002).

[4] J. Kedzierski *et al.*, IEEE Trans. Electron Devices **50**, 952 (2003).

[5] R. Chau *et al.*, *IEDM Tech. Dig.*, 621 (2001).

[6] T. S. Drake *et al.*, Appl. Phys. Lett. **83**, 875 (2003).

[7] K. Rim *et al.*, *IEDM Tech. Dig.*, 49 (2003).

[8] J. D. Bude, *Proc. SISPAD*, 23 (2000).

[9] F. M. Bufler and W. Fichtner, IEEE Trans. Electron Devices **50**, 278 (2003).

[10] C. Jungemann and B. Meinerzhagen, in *Proc. ESSDERC*, 9 (2003).

[11] R. J. Luyken *et al.*, Solid–State Electron. **47**, 1199 (2003).

[12] A. Svizhenko and M. P. Anantram, IEEE Trans. Electron Devices **50**, 1459 (2003).