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Silicon Nanowire Esaki Diodes

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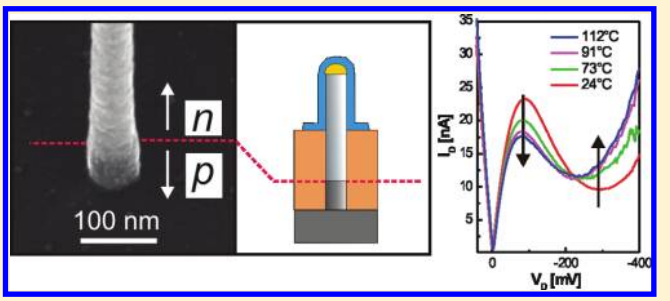
ABSTRACT: We report on the fabrication and characterization of silicon nanowire tunnel diodes. The silicon nanowires were grown on p-type Si substrates using Au-catalyzed vapor−liquid−solid growth and in situ n-type doping. Electrical measurements reveal Esaki diode characteristics with peak current densities of 3.6 kA/cm^2, peak-to-valley current ratios of up to 4.3, and reverse current densities of up to 300 kA/cm^2 at 0.5 V reverse bias. Strain-dependent current−voltage (I−V) measurements exhibit a decrease of the peak tunnel current with uniaxial tensile stress and an increase of 48% for 1.3 GPa compressive stress along the ⟨111⟩ growth direction, revealing the strain dependence of the Si band structure and thus the tunnel barrier. The contributions of phonons to the indirect tunneling process were probed by conductance measurements at 4.2 K. These measurements show phonon peaks at energies corresponding to the transverse acoustical and transverse optical phonons. In addition, the low-temperature conductance measurements were extended to higher biases to identify potential impurity states in the band gap. The results demonstrate that the most likely impurity, namely, Au from the catalyst particle, is not detectable, a finding that is also supported by the excellent device properties of the Esaki diodes reported here.



KEYWORDS: *Nanowire, Esaki, tunneling, diode, silicon, strain, phonon*

Ever since Esaki demonstrated the first semiconductor p−n tunneling devices characterized by negative differential resistance in forward direction,[1] many investigations were made to understand and improve the device performance. The fabrication of Esaki diodes requires the most stringent control over doping profile and crystal perfection and therefore constitutes an ideal platform to evaluate the junction quality using the peak-to-valley current ratio (PVCR) and peak current densities (PCD) as figures of merit. The metal-alloying process[2] used in the 1960s produced Esaki diodes of macroscopic dimensions with spike-like p−n junctions and resulted in excellent PVCR and PCD values that for a surprisingly long time were unrivaled.[3] Only with the emergence of advanced molecular-beam epitaxy techniques could silicon (Si) tunnel diodes (TDs) be fabricated in a more controlled manner, and only very recently were high-quality SiTDs produced that exhibited even higher PVCRs than those of the Esaki diodes of the 1960s.[4] Here we report on the fabrication and characterization of Esaki diodes based on Si nanowires (NWs) which are grown using the Au-catalyzed vapor−liquid−solid (VLS) method and which achieve high PVCR, high PCD, and high reverse-bias current densities.

Although the first report on a Si diode fabricated by VLS growth and in situ doping dates back to 1967,[5] no further work toward a SiNW tunnel diode has since been reported. The main reason is the lack of a suitable p-type dopant that can be incorporated into the SiNW core at a sufficiently high concentration and low growth temperatures. In our growth system, the doping level attained using diborane (B_2H_6) is limited to below 5×10^{18} cm^{-3} because of the limited solubility of B in Si at the VLS growth temperature. In addition, no incorporation of B using trimethylborane (TMB) even at a SiH_4:TMB ratio of 1:2 was detected. We circumvented these constraints on the p-type doping by directly growing n-type doped SiNWs using monosilane (SiH_4) and phosphine (PH_3) on degenerately doped p-type Si ⟨111⟩ substrates. From previous work,[6] we established a maximum attainable n-type doping concentration in SiNWs of 1.2×10^{20} cm^{-3}. However, as the nucleation yield and growth of epitaxial SiNWs are strongly reduced at these PH_3 concentrations, we set the PH_3:SiH_4 ratio to 1:420, which resulted in a nominal donor concentration of 1×10^{19} cm^3 in the SiNWs. All SiNW devices were grown in a cold-wall reactor at a pressure of 25 Torr in hydrogen. The substrates were ramped within 60 s from room temperature (RT) to 470 °C and exposed to 1000 sccm H_2, 3.2 sccm SiH_4, and 2.5 sccm of 0.3% PH_3 diluted in He. The Si substrates were prepared by BHF cleaning followed by deposition of 60 nm diameter Au catalyst particles from an acidified (BHF) colloidal solution. Then they were immediately loaded after rinsing in H_2O and blow drying in N_2. Figure 1A shows a scanning electron micrograph (SEM) of the sample after growth. Approximately 1.5 μm tall vertical epitaxial SiNWs are observed, but also kinked wires and not nucleated seed particles are visible. The kinked SiNWs were removed

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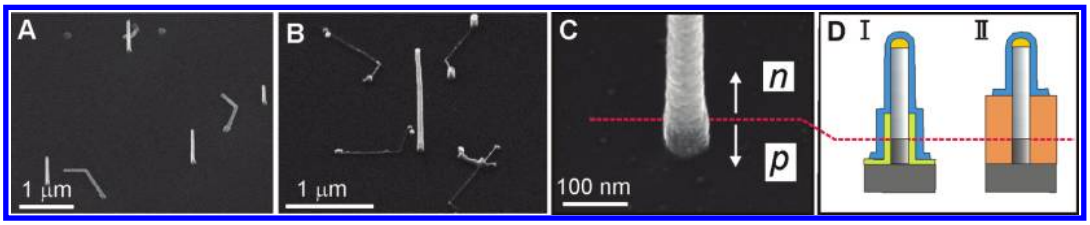

Figure 1. Fabrication steps of SiNW tunnel diodes on a p-type Si ⟨111⟩ substrate. (A) SEM showing randomly placed and epitaxial n-type SiNWs after the VLS growth (tilted view). (B) Image taken after anisotropic dry etching of 80 nm silicon. All nonvertical standing SiNWs were selectively removed in this process. (C) Close-up of a SiNW base, in which the p−n junction is situated 80 nm above the wafer surface. The diameter of the SiNW is approximately 60 nm. The red dashed line indicates the position of the p−n junction. (D) Schematics of the SiTDs fabricated: For one structure (type I), 20 nm of Al_2O_3 was deposited as the isolating material between the top contact of the NW and the Si substrate, whereas for the second structure (type II), 500 nm of the organic material, namely, benzocyclobutene (BCB), was used. Ti/Au serves as contact layer in both types of devices.

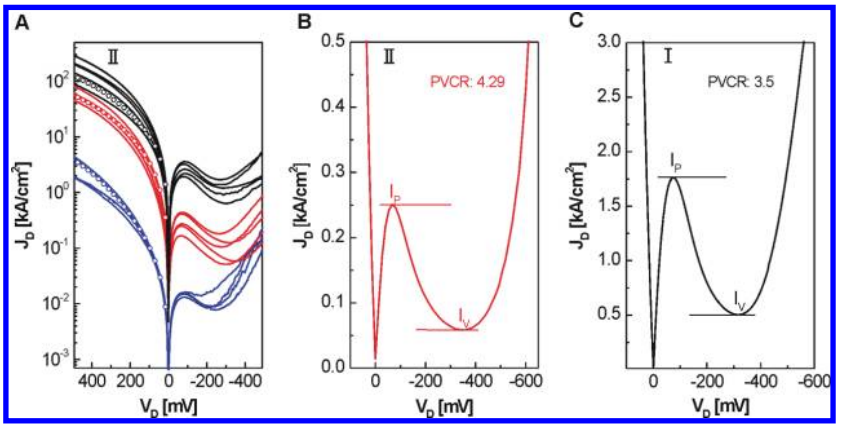

Figure 2. $J-V$ characteristics of silicon Esaki diodes. (A) The three data sets shown correspond to varying doping concentrations in the p-type substrate: 6×10^{19} (bottom, blue curves), 9×10^{19} (middle, red curves), and 1.2×10^{20} cm^{-3} (top, black curves), respectively. The three curves in reverse direction (open symbols) are simulated devices using a n-type concentration of $(5-6) \times 10^{19}$ at the SiNW junction. (B) Selected device from the middle data set of figure (A) with the highest PVCR of 4.3. (C) Type I device with a p-type doping of 1.2×10^{20} cm^{-3}. The growth conditions of the phosphorus-doped SiNWs were kept constant in all cases. The device type is indicated by the roman letter (I or II) in each panel.

selectively using an anisotropic Si dry-etch, as illustrated in Figure 1B. After the nominally 80 nm deep etch, only vertical SiNWs remained, with remains of the nonvertical wires leaving some marks on the surface. Figure 1C shows the resulting 60 nm diameter p−n junction located at the base of the SiNW. Two sets of control devices were also fabricated: In one set, Au was removed from the SiNWs using a KI etch, whereas the second set did not undergo any further dry etching. Both sets of control devices exhibit similar device characteristics as those that had undergone the Si dry etch. For the detailed study, we built two types of device structures according to the schematic in Figure 1D. Devices of type I use a 20 nm thick Al_2O_2 insulation layer to separate the anode and cathode contact, whereas devices of type II possess a 500 nm thick benzocyclobutene (BCB) layer. The Ti/Au metal contacts were deposited by electron-beam evaporation and lift-off technique. Electrical characterization of the diodes was performed in the temperature range from 4 to 390 K. For the measurements above RT, the metal pads were directly contacted by probe tips, whereas for cryogenic measurements, the pads had to be wired and mounted onto a chip carrier. Optical inspection was used to ensure that only a single SiNW is contacted by the probe pad. The SiNW diodes were biased at the n-type doped nanowire source side with the p-type Si substrate fixed at ground potential, defining the negative voltage as forward bias.

Current density−voltage ($J-V$) curves of three sets of diodes with varying substrate doping concentration of 6×10^{19}, 9×10^{19}, and 1.2×10^{20} cm^{-3}, respectively, are shown in Figure 2A. All SiNW tunnel diodes exhibit a negative differential region in forward bias, and both the peak and the reverse current increase with increasing substrate doping. The device variability observed in each set of data is attributed to differences occurring in the SiNW nucleation process itself. This process is expected to have a strong influence on the doping level and the junction width and thus significantly affects the tunnel current measured. Another source of variability is the diameter variation of the SiNWs, which can range from 50 to 90 nm and stems from the merging of Au seed particles during the deposition process. The small dimensions and geometry of the SiNWs inhibit chemical analysis for dopant profiling of the p−n junction by secondary ion mass spectroscopy (SIMS) and transmission electron microscopy based analytical techniques. However, this analysis might become possible in the future by applying more sensitive techniques, such is atom probe tomography. Therefore junction analysis is currently restricted to $I-V$ measurements and simulations.

For an electrical characterization of the p−n junction, PVCR is a well-suited figure of merit because it is strongly influenced by the level of excess current, which is linearly dependent on the density of trap states in the silicon bandgap. Hence, PVCR indicates how many crystal defects, i.e., dislocations or deep-level impurities, are located in the vicinity of the tunnel junction

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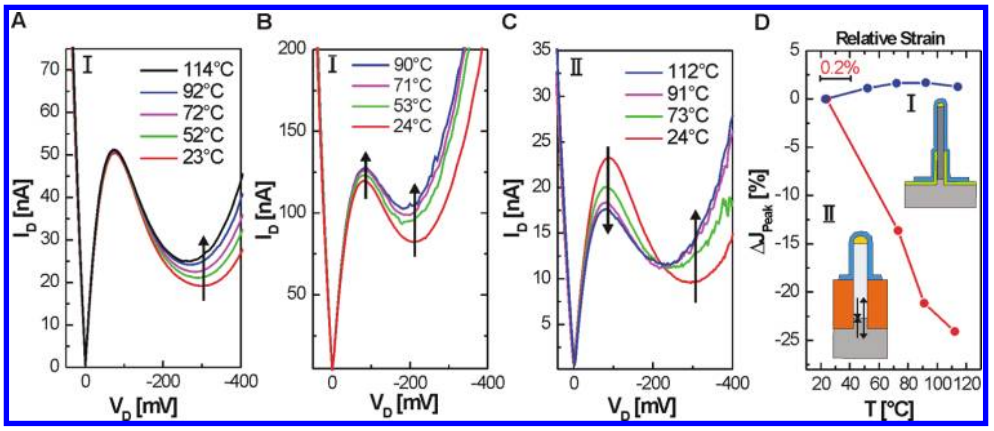

Figure 3. Temperature and strain dependence of SiNW tunnel diodes of type I and II. (A) The $I-V$ characteristics of a diode with a PVCR of 2.63 at RT illustrate how the excess current increases with temperature, whereas the peak current remains constant. (B) Tunnel diode with a lower PVCR of 1.5 at RT exhibits the same behavior of the excess current as the device in (A), but in addition the peak current increases with temperature. (C) Tunnel diode with a PVCR of 2.3 at RT shows the expected increase in excess current with temperature, but a decreasing peak current due to stress. (D) Comparison of the relative change in peak current density with temperature (strain) of the two device types. The relative strain for device I is indicated in the upper axis. The device types are indicated by roman letters (I or II) and sketched in the insets of (D).

and therefore contribute to the electron transport. The PVCR values derived from the $J-V$ plots shown in Figure 2A range from 1.16 to 4.3. For the diodes with a p-doping of 1.2×10^{20}cm^{-3}, the PCD values range from 1.9 to 3.6 kA/cm^2, whereas the reverse bias current at 0.5 V spans values between 90 and 300 kA/cm^2. Despite the lack of SIMS profiles of the boron and phosphorus distributions across the junction, we can conclude from the excellent electrical characteristics that the phosphorus doping concentration at the tunnel junction is significantly higher than that in the remainder of the n-doped ($N_D = 1 \times 10^{19}$ cm^{-3}) nanowire. This difference can be attributed to the higher incorporation of P during the nucleation phase compared to the steady-state growth regime. The lower limit of the donor concentration is set by the supply of P during growth, whereas the upper limit is given by the equilibrium solubility concentration of P in Si at the growth temperature, which is expected to be around 1×10^{20} cm^{-3}.[6] Using TCAD simulations[7] with a calibrated nonlocal band-to-band-tunnel model for Si,[8,9] the best fit of the experimental data set was achieved using a SiNW doping level at the junction of $N_D = 6 \times 10^{19}$ cm^{-3} for the highest-doped substrate and $N_D = 5 \times 10^{19}$ cm^{-3} for the medium-doped substrate. A good fit to the lowest-doped substrate with $N_D = 5 \times 10^{19}$ cm^{-3} was only possible by adjusting the substrate doping to $N_A = 3 \times 10^{19}$ cm^{-3}. Based on the measurements and the simulation, we conclude that the tunnel-diode structures consist of an acceptor region that depends on the choice of substrate doping, a thin space charge region, and a donor level in the range of $N_D \sim (5-10) \times 10^{19}$ cm^{-3} at the nanowire side of the junction, with the remaining part of the SiNW doped to $N_D = 1 \times 10^{19}$ cm^{-3}.

The combination of a high PVCR of up to 4.3 and concurrently a high PCD of up to 3.6 kA/cm^2 makes these devices among the best-performing Si Esaki diodes reported so far. The observation of such high PVCRs is surprising considering that phosphorus doping is known to result in lower PVCR than in arsenic (As) and antimony (Sb) doped devices because of its higher density of gap states.[10] Accordingly, devices with the highest PVCR have so far been fabricated using As doping[3] and more recently also Sb doping.[4] Whether Sb doping of SiNWs[11] can be used to increase the PVCR remains to be tested.

All diodes presented in Figure 2A were of type II. The $J-V$ curve of the diode with the highest PVCR of 4.3 in Figure 2A is displayed in Figure 2B on a linear scale, and a type I device with a PVCR of 3.5 is shown in Figure 2C. This demonstrates that both types of devices achieve similar performance in terms of both PVCR and PCD for equal substrate doping at RT. In addition, alterations of the junction characteristics in type I devices by electrostatic gating from the adjacent electrode can be excluded. However, when the operating temperature of the device is changed, it will matter whether an organic or an inorganic dielectric is used as embedding material because their thermal expansion coefficients differ considerably. Type I devices, with Al_2O_3, exhibit a thermal expansion of the same order of magnitude as that of Si, whereas type II devices have an organic dielectric with an effective thermal expansion of ~90 ppm/°C from RT up to 120 °C.[12] This is about 2 orders of magnitude larger than that of Si. Therefore, diodes of type I should show a normal tunnel diode temperature dependence, whereas type II diodes are expected to exhibit an additional stress dependence due to the thermal expansion/compression of the organic layer. In Figure 3, the two device structures are compared and evaluated in terms of temperature and strain effects. Figure 3A,B shows the temperature-dependent $I-V$ curves of two type I diodes, namely, that of an Esaki diode with a PVCR of 2.5 at RT in Figure 3A and for a diode with an RT PVCR of 1.5 in Figure 3B. The two data sets illustrate the different temperature dependences of the peak current observed for type I diode structures: The peak current remains nearly unaffected if the PVCR is large enough such that the low-bias tail from the (trap-assisted) excess current is much lower than the (phonon-assisted) tunneling current (Figure 3A) but increases for the low-PVCR device (Figure 3B) along with the temperature-dependent excess current.[13,14] In contrast, the characteristics of a type II device exhibit a more pronounced temperature dependence and a different behavior of the peak current (see Figure 3C). Here the peak current decreases by 24% with increasing temperature despite the increase of the excess current. However, as the peak tunnel current should increase with temperature because of the reduced band gap (E_g) rather than decrease, this drop can be attributed to mechanical strain acting on the tunnel junction.[15] The tunnel current depends on E_g and the effective mass,[16] and

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both increase because of the uniaxial tensile stress arising along the ⟨111⟩ direction. Figure 3D summarizes the temperature dependence of the relative peak tunnel currents of the diodes shown in Figure 3A,C. For the type II diode, we use a relative strain axis because we cannot accurately determine the temperature leading to zero stress condition in that device.

The influence of uniaxial compressive stress on the peak tunnel current was explored by cooling a type II device down to 4.2 K. Figure 4 compares the $I-V$ characteristics measured at

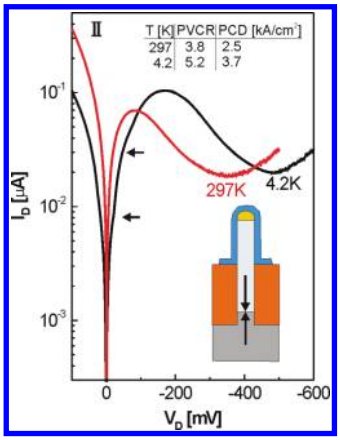

Figure 4. $I-V$ characteristics of a SiNW Esaki diode at RT and 4.2 K. The peak current increases by 48% due to a temperature-induced compressive stress in the SiNW tunnel junction. The shift between the two curves is caused by a higher contact resistance at lower temperature. The device figures of merit are listed in the upper inset; the lower inset shows the device schematic, with the vertical arrows indicating the strain applied to the junction. In the LT $I-V$ characteristics, two kinks at small negative voltages are apparent (arrows) that indicate the contributions from phonon-assisted tunneling.

RT and at 4.2 K. At low temperature (LT), the peak tunnel current increased by 48%, whereas the valley current remained unchanged, resulting in a rise of the PVCR from 3.8 to 5.2. This observation differs from the strain-free behavior of a Si Esaki diode, in which the peak current was shown to drop by 30−60% upon cooling of the device,[10,13] a behavior that mainly resulted from the increase of E_g with decreasing temperature. Consequently, the large increase in the peak current of the device shown in Figure 4 originates from a strain-induced decrease of the Si bandgap. This demonstrates that we can tune the mechanical stress in the device from tensile to compressive by adjusting the temperature, as expected from the difference in the thermal expansion coefficients of the insulating spacer material. From the thermal properties of the spacer materials used, a compressive strain of 0.7% in the ⟨111⟩ direction can be estimated, corresponding to an uniaxial pressure of 1.3 GPa at the junction. The strain-induced change of the bandgap $\Delta E_{g,strain}$ can be calculated based on the theoretical and experimental values for the pressure dependence of the bandgap of 0.11 and 0.14 meV/MPa, respectively,[17] which yields values of $\Delta E_{g,strain}$ from −143 to −182 meV.

Literature values of the bandgap in heavily doped Si span from 0.92 to 1.05 eV at RT and increase at LT by about $\Delta E_{g,temp}$ = 60 meV[16,18,19] Knowing $\Delta E_{g,temp}$, we can obtain $\Delta E_{g,strain}$ by a linear extrapolation based on the observation of the tunnel current reduction of a 30−60% of the unstrained reference devices from refs 10 and 13 and the 48% current gain in the strained diode, which results in a strain-induced bandgap reduction $\Delta E_{g,strain}$ of −108 to −156 meV.

Overall, the above analysis shows that the strain-induced reduction in E_g based on the compressive strain estimate of 0.7% matches fairly well with the measured current gain of 48%. We note that although a similar analysis is possible for the device under tensile strain (Figure 3C), it will be less favorable because the contribution of thermally activated excess current to the peak current can lead to an underestimation of the strain-induced current change and therefore of $\Delta E_{g,strain}$.

Figure 4 also reveals that the valley current of this device does not decrease when the temperature is lowered to 4.2 K, in contrast to what is usually observed and exemplified by the device shown in Figure 5. This suggests that the excess current

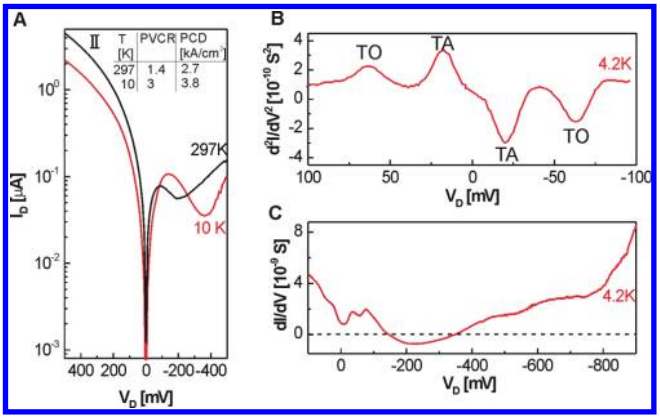

Figure 5. $I-V$ and conductance measurements of a SiNW Esaki diode. (A) Comparison of the $I-V$ characteristics at RT and 10 K. The shift between the curves results from a larger contact resistance at low temperature. (B) The second derivative of the current with respect to the voltage exhibits conductance peaks at the energy of the TA and TO phonons. (C) Conductance measurement at 4.2 K toward higher excitation energy. Whereas the contribution from TA and TO can be clearly observed at low bias, the smoothness of the curve at higher bias indicates a uniform distribution of defect states in the gap. Trap states from potential Au impurities are not detected.

in the device having a RT PCVR of 3.8 is not limited by thermally activated trap levels, as opposed to the device in Figure 5 with a PVCR of only 1.5.

The shift in the forward and the reverse bias direction between the two curves can be explained by an increase of the contact resistance between the Ti/Au metallization and the nanowire at low temperature. Another behavior observed in several samples, but not further investigated here, is the onset of electrical noise in the excess-dominated current, whereas in the peak current region almost no noise is detected. This phenomenon might be related to the small area of our tunnel junction and the finite number of defects that participate in the trap-assisted tunneling process. A closer look at the LT trace in Figure 4 also reveals two kinks at low bias in the forward tunnel direction, which originate from electron−phonon interactions that are required for tunneling in Si because of its indirect bandgap.

Tiny changes in the conduction can best be measured using a lock-in technique to record the second derivative of the current with respect to the voltage. In this way, the emission of phonons in the indirect tunneling process can be revealed,[20] as shown in Figure 5. The RT and corresponding LT $I-V$ plots of a type II diode are shown in Figure 5A. A similar behavior as

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reported for the device in Figure 4 is found, but in addition, a lower excess current is observed, resulting in an improved PVCR at LT. Figure 5B shows the second derivative of the current from 100 to −100 mV bias voltage. Using the second derivative of the current, a change in the slope will result in a distinct peak. Two peaks that are symmetric around zero bias are visible, which correspond to the energy of the phonon modes that couple strongly with the tunneling electrons, i.e., the transverse acoustic (TA) and the transverse optical (TO) modes. The peaks are positioned at slightly higher biases (19 and 63 mV) than the literature values of ±18 (TA) and ±57 mV (TO).[20] It is tempting to use the observed upshift in phonon energies to directly quantify the strain[21] in the nanowire. However, in our current setup, the aforementioned contact resistance of our device and the limited signal intensity would hamper such an analysis. Apart from phonon contributions, also trap states located in the forbidden energy gap can contribute to the forward current. If trap states are available, they can be identified by their energetic signature. Of particular interest in our case are levels associated with Au impurities introduced during the Au-catalyzed VLS growth of the SiNWs. We performed measurements of the second derivative toward higher bias, but these were limited by the signal-to-noise level. However, the less demanding conductance measurement could be applied instead (Figure 5C). The TA and TO phonon peaks are reproduced at low bias, but no pronounced structures are resolved at higher energy up to the onset of the thermal diode current. A broad peak in the excess current for Au-doped Si[22] and Ge[23] tunnel diodes in the $I-V$ curves was found, and distinct signatures of Au traps could be revealed by using derivative measurements at Au concentrations above 2×10^{16} cm^{-3}. We do not observe these effects in the $I-V$ curves or in the derivative measurements. From this, we deduce that the Au density in the junction must be significantly below 2×10^{16} cm^{-3}. As the PVCR and excess currents in our devices are as good as or better than those of the reference devices from[22] or devices made by MBE,[4] we conclude that the Au level *in* the tunnel junction is negligibly low (limited by the temperature-dependent solubility of Au in Si during SiNW growth) and has no influence on the device properties despite the fact that Au clusters on the surface of the nanowires can be detected by SEM.

CONCLUSIONS

In conclusion, we have demonstrated a novel method to fabricate Si Esaki diodes based on VLS growth. With a diameter of 60 nm, they are the smallest reported Si Esaki diodes. They exhibit excellent device properties with respect to both PCD and PVCR. Differences in the thermal expansion coefficients of the SiNW diode and the surrounding dielectric were used to probe the reversible thermomechanical response on the tunnel current. The only weak temperature sensitivity of the peak tunnel current enabled the discrimination and quantification of the silicon bandgap reduction caused by the compressive uniaxial stress. LT electrical measurements were conducted in a single SiNW junction, and the phonon energies from the TA and TO modes could be detected. Finally, tunnel spectroscopy was used to search for distinct trap levels in the bandgap. These measurements together with the excellent PVCR indicate that no trap states from Au impurities are present in the transport mechanism. Improvement in the sensitivity of the electrical measurements might make it possible to determine the pressure-induced phonon peak shifts and thereby enable a quantification of applied strain.

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