Eidgenössische Technische Hochschule Zürich
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Institut für Integrierte Systeme
Integrated Systems Laboratory

Department of Information Technology and Electrical Engineering

VLSI III: Test and Fabrication of VLSI Circuits

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Exercise 3

Tester Demo

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Reminder:
With the execution of this training you declare that you understand and accept the regulations about using CAE/CAD software installations at the ETH Zurich. These regulations can be read anytime at `http://eda.ee.ethz.ch/index.php/Regulations`.

1 Introduction

In this training, you will have your first encounter with the IC tester Advantest SoCV93000, which is located in ETZ J71.1. As you have learned by now in the lecture, this our primary equipment to test the chips we designed at our lab after we get them back from fabrication.

This training gives you a first overview of how to use this sophisticated piece of equipment. You will work through a full test procedure with a completely given test setup in order to get a first impression. In the upcoming trainings you will have a detailed look at the individual steps required to setup the device and the various functions it provides.

The learning goals of this training are:

- Learn how to turn on/off the device and how to install the tester boards.
- Learn how to properly handle chips, such that you do not destroy them even before you can put them on the tester.
- Learn how to use the basic functions of the tester software.
- Get the *big picture* of how this device is used and what can be done with it.

2 Preparations

You can find detailed manuals for the tester on our eda-wiki[1]. To prepare for this exercise, read the following pages: *Tester: Basic Handling* and *Tester Software*.

3 During the Training

Student Task 1: Preparations:

- Take ESD protection measures.
- Login to the hava workstation with your vlsi3 student account.
- Prepare the tester for testing with the `soc_ETH-CH_generic` load board and the `Student_QFN40.std_v1_rev0` test board.
- Run the install script to copy the data required for this training to your account. It will create a directory `ex_03` with all required files. You can also find in the folder the documentation of chip we are testing in this training.

```
sh> /home/vlsi3/ex_03/install_ex03
```

- Have a look at the `ex_03` folder. Also have a look at the datasheet of the chip we are going to test.
- Open the test software and load the existing *device* provided in the `ex_03` folder. Load the `isscc.oppower.artemis` test flow and open it.

[1] `http://eda.ee.ethz.ch/index.php/Tester`

Student Task 2: Test a chip with the given test flow:

- Determine if the tester is connected. Connect the tester.
- Run the continuity and the atpg test.
- Load a chip onto the tester. Which two things do you need to consider?
- Rerun the continuity and the atpg test.
- Run the remaining tests in the flow one after each other. Discuss the function of each test.
- Understand the test flow.
- Report a few performance figures and compare them with the provided datasheet.
- Change the chip. Which two things do you need to consider?

Student Task 3: Cleaning up:

- Close all programs and properly turn off the tester.
- Log off from the workstation and clean up the workspace.
- Do not forget to remove the ESD strip from your feet!

4 Discussion

Discuss the following points with your assistant:

- What is the most important point to consider when handling chips.
- Explain the different states (docked/undocked, connected/unconnected) of the tester.
- Elaborate the term 'device' with respect to the tester software.